GE research: Silicon compilation in days

A team from General Electric Research and Development Center has developed an advanced silicon compiler that drastically reduces the time it takes to design custom IC chips for the company's products.

The compiler was first used on two chips, both of which are 1.25-micron CMOS devices. One contained 33,000 transistors, while the other contained 15,000. The computerized tool completed the design cycle—from algorithm description to layout—in three days. With low-level compilers or assemblers, the development time would have been from six to eight months.

The chips are to be used in high-performance graphics computation. One chip had 1500 transistors per square millimeter—invoking what is believed to be the highest density layout for compiled nonmemory chips at this feature size. Interconnection wires occupy 10% of the total area, with wasted area at less than 1%.

With the compiler, chip design is generated directly from the specifier's high-level language description of the algorithm that the circuit will execute. Rather than detail how the circuit should operate, the description spells out what the circuit is to do.

The GE compiler language, which represents C, is designed for non-specialists, with emphasis on efficiency. The 35,000-transistor chip was fully specified in 100 lines of code.

Once the chip is specified, the compiler does a simulation to test the algorithm it has been supplied. This simulation produces data that mirrors the output of the eventual chip, enabling the designer to see how closely the algorithm achieves hoped-for results.

After the algorithm description is adjusted (if necessary) and certain housekeeping chores, such as defining the chip's aspect ratio, are completed, the design tool automatically compiles the chip. The system draws from its library of basic building blocks, such as adders, subtractors, and delay, to create the necessary specialized cells. It then determines how to lay out and interconnect the cells, following tried and proven design rules. It has built-in optimization routines designed to maximize layout density and minimize wire length.

The last step is to run the compiler's resulting chip description through a Calma workstation. In this process, the cell becomes detailed. The required transistors and other basic circuit elements are drawn in. The file from this process is sent to the vendor to produce the mask set needed for fabricating the chip.

As currently configured, the GE compilation tool is designed for generating circuits using a bit-serial architecture. This accommodates many digital signal processing applications required by GE's internal product operations. The design tool is fully functional at the GE R&D Center.

Prototypes of the two chips have been fabricated using GE's 1.25-micron, double-metal CMOS process. Both showed full functionality at first silicon.

ATE training

Lexico Enterprises is offering training from April to June, either on-site or at their facilities. Topics include Atlas digital testing, HP DTS-70 (offered separately for operation, use, maintenance, and advanced applications), Atlas (MATE) programming, and introduction to MATE.

For information on dates and prices, contact Barbara Thomas, Lexico Training Div., 19102 N. Creek Pkwy., Suite 106, Bothell, WA 98011; (206) 483-TEST.
GenRad completes largest order in history

Every tester company should have GenRad’s problems. After all, shipping 775 diagnostic test systems to Jaguar Cars in Coventry, England, was no easy matter, but somehow the company managed. The order—totaling $13 million—was the largest in GenRad’s 71-year history.

The JDS (short for Jaguar diagnostic system) was based on GenRad’s 2610 portable test system, and all diagnostic testing routines were derived from system application software developed by Cirrus Designs a subsidiary of GenRad.

Jaguar needed a means to test the seven microcomputer modules in its X140 models, which have recently debuted in the European auto market. The module included control timing, logic control, engine management, instrument panel, air conditioning, cruise control, and antilock braking.

The system had to be user-friendly for interaction with auto mechanics, so GenRad gave the JDS a hand-held keypad and simple menus that respond to one keystroke.

JDS starts the diagnosis with a series of questions on vehicle type and configuration, as well as on the nature of the fault. The system then uses the answers to determine the most efficient diagnostic procedure for locating the fault condition.

Graphics are used to illustrate information relevant to the problem. The operator sees only what is useful while locating the fault. JDS advises on which component needs testing and graphically depicts its location in the vehicle.

The database contains the color, shape, and position of every connector and the color of every wire. The process guides the operator through the optimum sequence, considering ease of access, until the fault is resolved to the lowest replacement unit (least expensive repair).

Translation is possible in six languages: English, French, German, Italian, Spanish, and Dutch.

The system uses a measurement probe, a current probe, and a set of hardware interface modules, called pods. The measurement probe measures voltage, resistance, and frequency. The current probe uses the Hall effect to make current measurements. Five types of pods are provided, including a utilities pod for continuity measurements and physical interface pods between JDS and the more complex microcomputer modules.

Motorola repeats design contest

Motorola’s E²-MC design contest, which ran during most of 1986, was offered as a challenge to engineers to develop innovative products using the MC68HC11—an HCMOS microcomputer with an on-chip EEPROM.

By popular demand, the contest will be repeated for 1987 with $10,000 in prizes.

For more information, contact your local Motorola sales office or an authorized Motorola distributor.

Rosy future for surface-mount packaging

Last year, IC package consumption in the US reached 6.6 billion units, with DIPs representing 84%. By 1990, however, DIP totals will decline to 63%, with surface-mount small outline packages representing 20% of the total.

Major growth is also forecast for ceramic chip carriers, and chip-on-board formats, according to VLSI-Era IC Packaging, an updated report from Electronic Trend Publications.

The report, which reviews the relative merits of each package type, finds that surface-mount packages are useful in VLSI ICs to reduce the performance degradation caused by through-board packaging.

The real problem stems from high-density VLSI ICs, which require packages with as many as 300 pins. The average DIP is available with as many as 68 pins, but is generally not practical beyond 40 pins. Chip carriers are available with as many as 124 pins, but are typically limited to 84. Pin grid array packages, currently the most practical solution to the high pin count problem, are not without attendant problems.

The report also discusses the move to on-shore assembly. Automated assembly, use of new packaging formats, and increased off-shore labor rates may mean that on-shore products can now be manufactured at lower cost with higher reliability.

The report costs $1500. Contact Electronic Trend Publications, 12930 Saratoga Ave., Suite D1, Saratoga, CA 95070; (408) 996-7416.

Laser modification of microcircuits

Lasertechnics has signed a technology transfer agreement with Sandia National Laboratories to develop a method for laser repair and modification of microcircuits.

The technology can be used to remove and insert microcircuit connections to correct errors in the initial design. The laser-induced cut and patch process may also be useful in producing custom-made microchips, such as small-volume application-specific gate arrays.

Lasertechnics plans to develop equipment that enables the use of this process for microcircuit fault analysis, prototype development, and yield enhancement.