1987 Editorial Calendar

Built-in self-test, fault analysis, manufacturing test, and ATE
With: “A Layout System for Custom VLSI” and “Testing Properties of PLAs”
Ad closing: March 1

April

Test Technology

Official DAC Issue
AT&T’s RISC microprocessor, Intel’s 8386, IBM’s Micro/370, and NTT’s 32-bit microprocessor
With: “The Effect of Modeling on Simulator Performance”
Ad closing: May 1

June

Physical Design

Special ITC Issue
Switch-level modeling, bridging faults, and detectable CMOS faults
With: “Parallel Probe Testing”
Ad closing: July 1

August

Switch-level Testing

October

CAD Parallel Processors

With: “Digital System Reliability,” “Chip-Level Modeling,” and “RAM Self-Test”
Ad closing: November 1

December

VLSI Layout

Submission: Send six copies of articles to Vishwani Agrawal, AT&T Bell Labs, Rm. 2C-476, 600 Mountain Ave., Murray Hill, NJ 07974. Send six copies of short papers to Sharad Seth, Univ. of Nebraska, Dept. of CS, Lincoln, NE 68588. Send department copy to Nancy Blackmon, Managing Editor, IEEE Design & Test, 10662 Los Vaqueros Circle, Los Alamitos, CA 90720.

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