ICCAD attendance up

The most recent version of the International Conference on Computer-Aided Design, held in Santa Clara, California, on November 10-13 wound up an unqualified success. The attendance of 1120 surpassed that of ICCAD 85 by about 10%, even in a time of tight travel budgets and generally smaller conference attendance.

ICCAD 86 was held in the newly opened Santa Clara Convention Center. The conference hotel, the Doubletree, opened only two weeks before the conference. Although there were the problems that one would expect with a new facility, hotel employees maintained a cooperative attitude.

Continuing the trend of past conferences, all tutorials were sold out even though, for the first time, attendance at the conference was required for tutorial attendance.

Attendance at the EDIF workshop, at 106, was down from last year's 150.

For the first time, ICCAD 86 formed two subcommittees for international participation: one for Asia and one for Europe. The chairmen of these subcommittees, Hajime Sasaki of NEC in Japan and Hugo DeMan of IMEC in Belgium, were members of the ICCAD 86 Executive Committee and oversaw the international review of all technical papers.

The total number of paper proposals for ICCAD 86 was 326, as compared with 248 proposals for last year's conference. Because of this increase and the high quality of the proposals, 115 papers were accepted, as compared with 101 last year.

The review procedures for the Technical Program Committee worked well, although next year, the committee plans to set up some way to explain why an individual paper was rejected.

The technical papers were expanded from three pages to four pages in conference digests, a change that proved popular among attendees. Authors should still submit full papers to the Computer Society, Circuits and Systems Society, and ACM/SIGDA publications.

Following the conference, a proposal was received from MCNC for ICCAD to sponsor a benchmarking meeting at ICCAD 87. Rather than formally sponsor such a proposal, the ICCAD Executive Committee approved MCNC to organize a meeting, on an experimental basis, for the Friday after ICCAD 87.

Insights from ICCAD 86

Charles E. Radke, IBM

Computers have evolved through three eras, according to ICCAD 86 keynote speaker, John M. Scanlon, in his presentation, “Computers for Communications—Or Is It the Other Way Around?”.

First there was the mainframe era, according to Scanlon, Group Vice President for AT&T's Computer Systems Division, which was brought on by the advent of the transistor, from the mid-1950s to 1968. Then there was the mini era, brought about by LSI technology, which reached its peak in 1978. Finally, there was the micro era, characterized by the personal computer, which started around 1979 and evolved from advanced technology, floppy disks, and standard operating systems—and which Scanlon claims has now reached its peak.

Each new era was created from reduced prices for entry-level computers and a new set of customers. Previously acquired products, however, were not replaced, and, in fact, each era's set of products continued to grow. Today, he stressed, the customer is intent on connecting equipment that is already available.

Communication barriers—data, voice, and imaging—have blocked any more PC penetration into white-collar work environments. Barriers are primarily in two areas: desktop to human communication and desktop to other computers. Individuals who must execute many tasks and who consider machines useful if they can be used with minimal training are a fertile market.

Scanlon offered several prescriptions for success. He advocated a world-wide numbering plan for electronic mail along with multitasking operating systems.

He stressed that many required capabilities already exist. Voice synthesis is largely available, and voice recognition is nearing commercial feasibility. Three-and-four-MIP micros are available (and RISC approaches extend that power to 10 MIPS). The touch screen is just about here, and transmission rates of 10 M bps over a twisted pair is possible. One cannot reach the customer, he explained, if all houses have to be rewired.

What, then, is holding back the fourth era? A greater level of silicon integration is needed, according to Scanlon, and millions of gates will be required to achieve needed communication functionality.

Scanlon concluded with a positive yet challenging note: “In spite of all the bad press, it's a good time to be with a computer company or a communications company, and it's a fantastic time to be with a company that's in both!”

Japan's fifth-generation effort

A description of the Fifth Generation Computer System project, which was given later in the conference, seemed to support Scanlon's characterization of computer industry evolution.
Hideo Aiso from Keio University in Tokyo and the chairman of the Steering Committee for the FGCS project talked in terms of 1000 GFLOPS or 1 million MIPS by the year 2000.

He characterized the FGCS as a system that focuses on processing and communication over local area networks of data, voice, diagrams, graphs, pictures, and words.

The implementation of an FGCS prototype machine requires three areas of concentration:

1. Hardware, including parallel processing and relational database machines (which he called “inference subsystems”)
2. Software, including program languages and basic software (which he termed “knowledge-based subsystems”)
3. Development support systems, including design tools.

fields under device gates result in carriers that start to reach saturation levels. Finally, mobility is degraded.

The thorniest problem, however, is the existence of hot carriers causing latch-up problems and electron velocity saturation.

Buss advocated three-dimensional integration to achieve future required levels of integration. He also concluded that innovative architectures would play a key role—even using today’s technology.

**The needle in the haystack**

In a panel on fault modeling, Vishwani Agrawal of AT&T Bell Labs offered a solution to the age-old poser “How does one find a needle in a haystack?” The solution, Agrawal said, is to “adjust the tool being used to the defect being looked for—that is, use a magnet instead of a flashlight.”

Although most researchers are still investigating logic-level testability analysis, apparently they are increasingly looking at device and interconnect levels associated with specific semiconductor processes.

John Shen from Carnegie Mellon University said that the peculiar defects of each semiconductor process must be known. One set of CMOS faults could be characterized as 52.5% breaks, 24.0% bridges, 19.4% transistor stuck, 1.2% transistor stuck-open, 2.6% a combination of breaks and bridges, 0.2% parasitic transistors, and 0.1% unexplained.

R. Walther of IBM summed up the opening discussion nicely by saying that if you cannot detect a particular defect—such as a CMOS bridging fault—then the solution lies in changing the design until the testability objective can be achieved.

The panel agreed that the amount of SPICE-like circuit simulation time was becoming excessive and that there is a need for statistical analysis and evaluation of testability against process characteristics.

**Not all is rosy at a half micron**

“How big is a micron?” was the focus of another conference session. Dennis Buss of Texas Instruments, in a plenary paper entitled “The Half-Micron Apocalypse,” provided an intriguing answer: “While we’ve been talking your fingernails grew five microns.”

Buss argued that half-micron feature sizes will be the limit for semiconductor products made with conventional technology. Four factors will create this limit:

1. performance degradation, where smaller does not mean faster
2. process control, where yield becomes a limitation
3. price competition, where the traditional profit motive plays a less important role
4. cash flow.

He indicated, possibly joking, that the last two factors are the dominant ones today.

Buss observed that NVIDs, or “not yet invented devices,” will be required to continue the historic advancements in semiconductor density and performance beyond one-micron feature sizes.

Why not MOS circuits below a half micron? There are several reasons. One is that depletion regions overlap, and problems of complexity arise. Another is that...
Ron Pinter of IBM-Israel provided insight into how the virtual grid approach reduces coding complexity.

**Compaction algorithms**

Chi-Yuan Lo of AT&T Bell Labs described MACS compaction. MACS is event-driven in that it focuses the compaction along the graph-critical paths in the circuit.

Ron Moore of Texas Instruments described Coordinator, a design-rule-enforced layout methodology, while Jeff Burns from UC Berkeley described a constraint graph spacer, called SPARCS, which can address the special problems of analog circuits.

**Benchmarking**

Tom Krakow from MCNC chaired a panel discussion on the role of standard benchmarks for comparing compaction.

Krakow started the discussion by outlining the current set of benchmark circuits and addressing the issues of metrics for comparing compaction techniques.

He also addressed the issues of interchange formats for design data and issues of technology choice. Wayne Wolf of AT&T Bell Labs suggested that the benchmarks should provide for a “shoppers’ guide” to compactors, and he expressed no sympathy for vendors unwilling to cooperate in benchmarking with commercial tools.

David Tan suggested that larger, more complex designs were needed along with analog examples. Tan also suggested that additional compaction constraints should be added, including fixed-aspect ratios, electrical area/speed performance, and design entry cost.

Chris Croes added that the ability to include a “dirty technology” would more critically test compaction as well as allow the comparison of compaction results to hand-crafted layouts.

Carlo Sequin suggested that larger and more irregular examples are needed to critically test the algorithms. He also suggested that EDIF be adopted as the standard interchange format for transmitting design data and sharing results.

Tom Krakow suggested that MCNC could act as a clearing house for running design rule checks on compacted results. He also suggested that CIF may be a practical interchange format for design data. A committee is being formed to address future plans in compaction benchmarking. Tom Krakow is the contact person for more details and release dates for the benchmarks (call (919) 248-1859).

**Concerns for the future**

The workshop concluded with a discussion that centered on the future of symbolic design in light of the new design automation tools available, which attack the design problem from a higher level. Examples are silicon compilers and logic synthesis.

Carlo Sequin believes that designers will learn to use compactors instead of mask editors, in the same sense that very few programmers code in assembly language given the availability of higher level languages such as C, Pascal, and Fortran.

Al Dunlop of AT&T Bell Labs presented a “wish list” of compactor features that included compactors with automatic jog insertion, analog circuit compactors, placement perturbation, design rule violation eliminators, and “whole chip” compactors.

Tom Lengauer proposed using compactors in two roles: as a clean-up tool for dirty layouts, and as the last tool used in a circuit generator system.

Yuki Watanabe of the University of North Carolina at Chapel Hill, speaking from the designer’s perspective, added that designers are not interested in the details of geometric rules. He believes that the symbolic layout is advantageous because it frees designers to concentrate on architectural issues.

VLSI Technology’s Chris Kingsley feels that symbolic layout’s time has come and gone, and designers will only use the tools if they can take poorly defined inputs and produce great layouts.

Neil Weste, on the other hand, argued that at Symbolics they are successfully designing large complex custom chips using symbolic layout and compaction. Weste stated that symbolic design is ideal if you have (1) short design cycles, (2) a limited number of designers, and (3) complex designs.

Steve Daniel of Thinking Machines pointed out that symbolic design techniques allow for parallel development of ICs and a foundry because the details of the technology are hidden from the layout.

The overall consensus from the discussion was that symbolic design has a place in the design process, but users will be reluctant to use such tools until they are integrated into a larger design system.

**Future workshops**

This meeting was the first in a series of focused workshops that MCNC is planning. The workshops will be structured to include formal presentations and a comparison of different approaches with standard benchmarks.

A workshop on logic synthesis with benchmarks is scheduled for May 12-15. A workshop on IC placement is scheduled for spring 1988.