D&T: Let's start with the vendor's view of the present situation. What are the key capabilities of today's testers?

Bisset: Well, that depends on what we think of as testing. There are obvious things like vector rate and megahertz and pin count, which are easy to determine. But in this context, most testers are about the same. If we look beyond that, we see significant differences in waveform fidelity, rise time, fall time, overshoot/undershoot, and cross-talk, for example.

We also need to consider whether the system is designed to operate in a terminated or unterminated environment, how accurate it is, and the minimum pulsewidth it can handle. We should also ask whether the equipment can test a part specification individually, or will it test all the specifications together under the assumption that they will interact at some point.

D&T: You won't always know the answer to that last question will you?

Bisset: No. For example, if you take high-speed parts such as ECL gate arrays, you may determine that it's adequate to initialize the part into a known state and then test for delay path propagation individually. A test system that can do that accurately may be less expensive than a system designed to exercise all aspects of the part at speed. And the more expensive system may not have any greater accuracy either.

So to sum up what I was saying, a number of current testers can test parameters in combination at 40 to 50 MHz and 256 pins. A couple of advanced systems are starting to handle the 100+ range, but in terms of what's deliverable, 40 or 50 MHz is realistic. Anything beyond involves some limitation, either in flexibility or types of chip/pin configurations you can use.

Roth: I agree. Most products can be tested with 40 MHz, 50 MHz and 256 or 288 pin count. Sure, a system here and there may need 120 MHz, but that's one special-purpose application. But the hardware capability is not the real issue. The real concern is how efficiently we program the system, and this depends on how strong our link is with the design world. This factor is influencing the way people view ATE.

D&T: So you're saying the system environment is more important than the tester's physical capability?

Roth: Yes, and I think also that the complexity of the devices being tested has a lot to do with system environment. There's far more engineering content in every new device than in the past. The concern is not so much with production; it's more with the amount of engineering needed.

If I'm developing a processor, for instance, I'm going to care about the difference between 10 MHz and 12 MHz because the market is so competitive. Engineers have to squeeze that extra megahertz out of every product. The fact that they're spending this much time on engineering makes it a key issue.

D&T: Do you see anything in your products that supports this?
Maruyama: Of course I agree that system environment is important. However, you can't diminish the importance of hardware. That's the real issue. Advantest's system offers 40 MHz with better than one nanosecond accuracy. Sometimes, because of multiplexing, it can generate up to maybe 80 or 100 MHz.

In my opinion, pin count is the key issue. The pin count capability could not feasibly be less than the device pin count. The test system must be viewed not as a computer system, but as a measurement tool, and this context should be given preliminary consideration. Then, testing environment factors such as programming, debugging, and networking can be considered. In other words, both areas are important, but you need to satisfy your hardware requirements first.

D&T: What is the current limit on pin count at high speeds?

Maruyama: Probably 256 pins. In 1988 or 1989, we'll probably need to accommodate devices with over 512 pins.

Griggs: I basically concur with what's been said. I think any one of the testers represented here can handle the common run of today's devices. What distinguishes a tester is its degree of flexibility. One of the things we can always count on is change. There's probably nothing else we can count on. So, when you pay $1 million to $2 million for a tester, you want something that's not going to be obsolete in a few years. You want a tester without bounds at 20 or 30 MHz, one that can go up to 50 or 100 MHz. You also want timing accuracy because you know that the timing demand is just going to increase.

D&T: What about gallium arsenide devices? We've heard some concerns as to whether today's testers can handle them. What do you think?

Bisset: It depends on the type of GaAs device you're talking about. If you mean the type that is designed to compete head to head with the ECL gate array, then the requirements for testers really don't change much. If you mean other applications that involve very high performance, limited pin count, analog or mixed analog digital functions, then the answer is we can't handle them. But that's not your average application.

Megatest has a customer that uses the tester on GaAs devices. These devices push the limits of deliverable speed and accuracy, but otherwise there's no difference.

Griggs: Sentry-Schlumberger's Sentry 50 has a mixed-technology test head, which handles 50 ohms, 100 ohms, TTL, ECL, and GaAs devices. I see a big difference in testing requirements in the high-end frequency. Some GaAs devices can get up to 400 or 500 MHz. I don't think anyone is ready to accommodate that.

What we can do realistically is go after as high a frequency as possible, usually in the 100 MHz range, sometimes 100+. Additionally, we have timing accuracy down around 20 ps for individual parts with 200 ps for the total system.

D&T: Okay, now it's the users' turn. What do you think of this assessment of current tester capabilities?

Barber: Well, for the most part, I agree. Just about any tester represented here could test most of today's products. As a user, I would probably base my selection on cost more than anything. I'd rather go for a $700,000 tester than one that costs $2 million. Also, personally, I insist on a workstation—Apollo or MicroVAX, whatever—with an Ethernet link to AT&T's CAD systems.

Additionally, at least at AT&T, a tester is generally selected for continuity with the systems already chosen, regardless of cost. We often stick with one manufacturer because we've trained lots of engineers on a particular system, and we'd have to start over with a new machine.

So basically I'm pretty satisfied with what's available now. If I had it to do over, I'd go with the lowest cost machine. Aside from price, they're all pretty much the same, probably because many tester designers drift from company to company. I know of one guy who went from Fairchild to GenRad to Megatest, for example.

I do see some serious problems in the future, however. IC design rules keep shrinking, and today's testers just can't handle them.

D&T: Anyone else?

Millham: I'm not entirely satisfied. From a manufacturing perspective, testers are dogs on throughput, particularly when you remember how much you pay for one. In a manufacturing environment, slow throughput is a major problem, especially when you're dealing with large structures, say LSSD, with deterministic patterns.

D&T: How large?

Millham: At about 10,000 to 20,000 gates, you start getting into trouble with today's systems. You have to reload the buffers, which causes a long delay in your test sequence. So, you just sit there and wait for the products to get through the machine. Also, setup times for the front ends can be long. Electrically, I have no argument—testers do a good job—but when you're collecting a lot of data, very often things tend to bog down.

D&T: Would that be parametric data or go/no go?

Millham: Parametric, also fail data for logic if you're trying to do a diagnostic afterward. You've got to collect large amounts of data in any case, whether parametric, fail, or logic, and you have to stop to do it.

Another thing, we need new machines for pseudo-random patterns and signature analysis, which, to my knowledge, nobody is providing except for some of the smaller board testers.

Barber: I don't quite agree with those comments about throughput. At AT&T, we have
been testing microprocessors that run with 100,000 test patterns. A number of tester companies have claimed that their machines can test faster, and they'll reprogram part of the test software. The result is throughput time that's about 10 times faster.

I know of other users who had the same experience, so we all sat down together and figured out that the tester companies had taken shortcuts that we ourselves could have taken if we'd known better. When it came right down to it, the test vectors dominated the test times, and they all came to about one second. Of course, you expect differences with data collection and dc measurements, but if you concentrate on functional test, throughput time is about the same for every tester.

D&T: You mean a vendor can help you tune your test program and ultimately speed your throughput?

Barber: Yes, some vendors have come in and shown us tricks, which we've used to change the program embedded in the test machines. We sped things up by 10 times, but it was simply that their test engineers were smarter than ours, not anything complicated.

Millham: I think you missed my point. Yes, testers are all pretty much the same on throughput, but what I wanted to come across with is that they're all bad.

Maruyama: Throughput to me consists of pattern generation and dc parametric testing. We have to load and reload after each pattern generation, which slows things down. Dc parametric tests are also taking more time as the pin count increases. This is a generic problem that has yet to be solved. For example, if the count is up to 1,000, the portion of total testing time is substantial. If the tester is designed to handle 100 MHz, the actual test time might be only 10% of the total time, with the rest being dc parametric testing.

When a high-speed tester is used for high-speed testing, the dc time becomes greater. However, for functional testing, there are several approaches to improving test speed, other than implementing a large buffer memory. One of these is to have accurate timing systems and many timing sets to avoid multiple runs of ac function test to check the critical path guaranteeing hold and setup time.

On a slightly different tangent, if a user insists on speed, which means real-time speed for the operational device, the cost will be high. Why not offer very accurate timing at a lower cost?

D&T: Okay, moving on, what additional tester capability will we need in the next five years?

Barber: At AT&T, we've been working with the present 40/80 MHz machines with silicon running down to 1.25 micron design rules, that is, 1.25 microns from source to drain. We are rapidly going to .7 micron devices in silicon, and we're going to see GaAs very shortly.

There, the speed is rapidly going up over 100 MHz. AT&T has a lot of optical communication circuits funneling into a 1.7-GHz fiber, so circuit frequencies are in submultiples of that. We happened to have several around 140 MHz. Also, some government projects are calling for 400 MHz. At those speeds, tester manufacturers aren't helping us.

What we're having to do is "turbo-charge" our slow, old 40/80 MHz machine by putting GaAs circuits on the load board. That way, we can sharpen the waveforms to get the frequency up.

Millham: It would be nice if, within a given tester company, we could see the same tester cover the span of chips, through cards and boards, possibly with a different front end for each.

Industry isn't really supporting the development of front-end interfaces, and as we increase frequency, we're going to hit the wall pretty soon. This wall won't be what tester manufacturers can produce; it's going to be what we can interface to the product. Maybe that's the user's job, maybe not. I think we strive for a combined effort.

D&T: Any vendors care to comment?

Roth: It will be very difficult for ATE suppliers to keep pace with high-performance requirements unless somehow they get help to achieve those milestones. Help means sharing the development costs or purchase orders, or something. Anything but what we're doing now, which is chasing after the higher performance ante. We need to make the user and the vendor very comfortable with each other so that they can work together to find a way to move forward.

D&T: What about the impending use of GaAs and the increased speed that it brings? Doesn't that give you a direction for your efforts?

Roth: How can we accommodate a GaAs device that needs to be checked at 2 GHz? We first of all need the technology. So somehow you have to be close to a GaAs company, and your relationship has to produce something down the road. How do you second guess when GaAs technology is really going to take off? We're still trying to reap the benefits of the 32-bit microprocessor market, and already we're being asked to anticipate GaAs. It's tough to justify in a business sense.

D&T: So where do you think you ought to take the development?
Bisset: I think where we should go is a straight line from where we are now. Look at the current level of testing requirements. Current tester architecture can handle all specifications of most parts. There are always exceptions that will be beyond the state-of-the-art tester, and we have to make compromises to get testing done a certain way. But basically, test system architecture can test all specifications except these special cases.

Now let's break down the test system requirements. One is the time to develop the software, and that encompasses computing cycles, workstations, and software structure. But most important is tester flexibility.

Megatek's tester per pin can translate waveforms specified in the part's design to waveforms that the tester can execute. The result is cycle by cycle, pin by pin independence of a sufficient number of edges. We designed the hardware with enough flexibility for the software to describe the testing, not what the tester does to do the testing. The result is you don't have to develop arounds to trick the tester into sort of testing the part. So the number one requirement is to translate the spec directly into the testing without compromise.

What you have to do now is improve the throughput. Tester manufacturers have practically eliminated the local memory buffer problem, and more recently they've tried other things like human intervention, programming shortcuts, and program optimization. But most of these aren't practical.

A better approach is to design the test system to execute from table-driven structured software. You build a test system from the ground up so that the most structured, most readable, most easily generated form of test program also executes in less than a second.

So if you have both flexibility and speed in your architecture, you can avoid modifying it significantly as you move up in speed and pin count.

If you build a system with "head room," both the customer and the vendor will save money. You provide a lot of initial detail like the amount of pipelining, the bandwidth, the interface between the mainframe and the test head, and whether you'll send both edges of a pulse out on a single wire or use two wires. Detail like that gives you mileage on old parts. Then, to cope with future requirements, you just shrink the tester architecture the same way you'd shrink a chip to make it go faster.

Gene Roth: "We need to make the user and the vendor very comfortable with each other so that they can work together to find a way to move forward."

D&E: Anyone else?

Griggs: I don't see 140-MHz GaAs devices as being any kind of problem for our tester. Of course, 400 MHz is another story.

Also, we at Sentry have an approach to help development from chips to cards to boards. This capability was established in a relationship with a customer in which we are not only testing chips, but also testing at the module level.

That wall between vendor and customer, which someone mentioned earlier, can be avoided if we maintain a close working relationship. I don't see a major obstacle in who provides what. All of that can be worked out.

One other point. I see definite performance differences in today's testers. Sentry's 550 can be expanded to 512 pins and 140+ MHz clock frequencies. Additionally, it can run at a straight-line test rate of 100 MHz. Above 100 MHz, we start giving up some functions.

Also, if you don't incorporate high accuracy from the ground up and control timing paths, you won't have an accurate end product. I believe that our accuracy is the best in the industry.

D&E: Now that all the users have heard the good things vendors are going to do in the future, do you feel more comfortable?

Barber: I don't. I have three points. First, I disagree that testers per pin are such a great deal. They're being pushed as providing high throughput and ease of programmability, but they're expensive. The same amount of money could be used to buy two tester systems instead of one. At AT&T, we use automatic test program generators, so we don't care if the system is easy to program. We can direct the output to a Sentry or a MegaOne or an Advantest machine; it makes no difference.

My second point is that most testers run at 40/80 MHz or 50/100 MHz in the return-to-zero mode. If you agree to go to a non-return-to-zero waveform, some testers can run double that. The Advantest machine, for instance, which is advertised at 40/80 MHz, will run at 160 MHz in NRZ format. The disadvantage is that NRZ may limit your testing capability.

My last point is that, historically, the vendor has always been way ahead of the customer in technology. When the customer had 10/20 MHz parts, the tester could always be made with 100K ECL to run up to 100 MHz. You seem to have topped out at 100 MHz though. Nothing can run over 100 MHz in the RZ format because of the ECL limitation.

In short, the users have gained on you with their submicron silicon and GaAs. They're now in the hundreds of megahertz. And it happened quite suddenly. I agree that we should be working closely together, sharing our technology to help you build those testers. I'm not sure you have access to the circuitry running at the higher frequencies.

Griggs: I agree, and without that access, I don't foresee us staying as far ahead as we did in the past.

Barber: One other point. Users really want a simple functional tester for high frequencies. We don't want programmable loads or even dc measuring capability really. Submicron MOS and GaAs parts are being designed to drive 50-ohm transmission lines, so as long as tester manufacturers provide a test head with a terminated transmission line running into it, I think that's enough. You don't have to build a complicated test head.

All the current testers are designed with either 50-ohm or 100-ohm transmission lines. Actually, I think all the new high-frequency circuits should be driving 100-ohm transmission lines because that means a smaller buffer on chip output. When you have to drive 50 ohms, you take up more silicon or GaAs area. But we seem to have inherited a 50-ohm history from ECL. I guess it's a standards problem that should be addressed by both the tester and the designer communities.
D&T: Does any user here feel comfortable about future tester offerings?

Millham: I don't, not really. I don't understand, for example, why manufacturers can't improve their buffer storage efficiency. Certainly at some point you've got to run out of steam. To my knowledge current machines have chips with only 10,000 to 20,000 circuits, not particularly big now and definitely small for five years from now.

You mentioned an architecture with up to four bits per pin per cycle. Now I'm looking at 10,000 to 20,000 circuits, and I'm looking at maybe 500,000 cycles of the tool at that many bits per pin per cycle. What I see is that I've got to ship an awful lot of bits around, either through the, the pad, the expression, big blue computer and/or the tester and I've got to store a lot of them. All of this takes time away from testing. I don't think you guys are addressing that problem.

Maybe you could look at ways to reduce the number of bits we've got to ship all over the architecture, and that might improve the throughput.

I also agree that we need a simple functional tester, not desire it, need it, for all the reasons mentioned. I'd love to have a general-purpose machine that lets me do everything at 500 MHz, but I think the probability of getting one is pretty slight. We're most likely going to end up testing the high-speed chips for parametrics on some dc tool off in the corner and then taking them to a high-speed tester.

Barber: Exactly.

Griggs: I'd like to show you the general-purpose 100-MHz capabilities of Sentry's S50.

Roth: As a vendor, I have no problem with separate paths for speed and dc parametric testing. We've been coming to you saying, "This is the only way we know how to do it." If you want a dedicated high-speed functional path, that seems like a reasonable compromise to me.

Maruyama: One of Advantest's customers wants to have a test system at 100 to 200 MHz, with about 500-ps accuracy, that can handle a pin count of 500+. That's a specific need, and we work to realize the appropriate hardware and software for that need. It involves particular compromises, but the result is something that is tailored for the application. We could not have done it without asking the customer specific questions, like what type of device is being measured and what is its speed. By working with the customer, we are able to optimize both throughput and cost.

Bisset: Getting back to the vector issue, it's an interesting calculation. Half a million vectors on a 200-pin system translates to 100 million bits of storage. If a DRAM costs $10 per megabit, the cost of the tester chips to store half a million vectors is $1,000. It's interesting when you consider how expensive the test system is.

My point is that memory is cheap, so it's not the real problem. Performance and signal fidelity tend to swamp issues of bit storage and moving costs.

D&T: In other words, the vendor must agree to look at some of the ways hardware is allocated and maybe choose other ways to save on timing, not so much on cost, because the cost of vector bits is relatively low?

Bisset: Yes. I think minimizing the hardware cost of higher speed and accuracy and maximizing test system throughput are much more challenging problems for test equipment manufacturers.

Barber: One last comment on the high-frequency challenge. As frequencies go up, test engineers seem to spend longer hours at the test system. Until recently, AT&T's test engineers were spending only about three hours at a session. In the high-frequency environment, it would be nice to have a tester assigned to an engineer for considerably longer.

D&T: But isn't that a development test activity?

Barber: Yes, but I predict that because of the subtleties of high-frequency problems, at 400 or 800 MHz, or even 140 MHz, engineers are going to be spending long hours at the test system. So we need low-cost systems. We can't afford to spend $2 million for a system and have one engineer tie it up all day.

D&T: What about a system with multiple test heads, so several engineers can work simultaneously to solve their respective problems, a sort of time-share arrangement?

Barber: That's a good idea, especially since each engineer would like to leave the tester set up overnight. That way, all the appropriate sampling scopes and auxiliary instrumentation don't have to be removed and set up again the next morning.

D&T: To close the discussion, I'd like to summarize what's been said. If we look at the hardware available in the current marketplace, in general it satisfies the customer's demands. There are special applications, but they don't drive the market, and they can be solved case by case.

As we go into the future with the higher speed GaAs products and requirements for higher pin count, it becomes a matter of economics in choosing the best way to satisfy the demand. Does a company try to solve all problems for all customers, or does it carve out a niche for itself in the market, solving only a particular class of problems? Yet another alternative is to get into some cooperative venture with a particular customer, provide something tailored to the customer's needs, and hope that other customers will have similar needs.

The future doesn't appear to be so bleak with all these alternatives. The process may be trying for both vendor and user, but that relationship is really characteristic of any growing business.