Intelligent control system to speed GaAs production

DARPA, through the US Army Research Office, has awarded General Electric’s Research and Development Center a $4.4 million contract to pioneer a computerized intelligent control system to speed commercial production of high-quality gallium arsenide crystals.

GaAs crystals are difficult—and therefore expensive—to grow at present. But discrete devices and ICs made from this material are critical to the development of advanced radar systems that operate at microwave frequencies and beyond, as well as high-speed electronics equipment and satellite communications systems capable of handling vast amounts of data.

The two-year contract will sponsor studies at the GE center, at Spectrum Technology, at Nektonics, and at GE’s Electronics Laboratory.

GE will provide expertise in computerized expert systems, factory automation and control technologies, and the manufacture of ICs that operate at microwave frequencies. Spectrum Technology will supply process expertise and facilities for demonstrating the advanced technology developed during the project. Nektonics will perform modeling studies and numerical simulations of the fluid mechanics and heat transfer behavior during the crystal growth process.

During the contract, an intelligent computerized control system will be developed and transferred to the commercial semiconductor wafer production line at Spectrum Technology.

Wafer material produced by the new process will be used to make monolithic microwave ICs at GE’s Electronics Laboratory in Syracuse, New York. The performance of these circuits will be a measure of the quality of the substrate material.

Robert C. Linares, president of Spectrum Technology, believes that the project will substantially reduce the cost of producing gallium arsenide, tighten the quality assurance methods used in production, and dramatically improve the product’s size, yield, and uniformity of electrical properties.

If the project succeeds, DARPA plans to have the team develop a full-scale production system that will provide high yields of wafers up to four inches in diameter.

A primary goal of GE researchers is to develop a sensor to monitor the crystal-growth process. The data provided by the sensors will be fed into a computerized controller, which will automatically take corrective measures if a minor problem develops.

Researchers also plan to develop a monitoring system based on a TV camera and infrared sensors. The system will be validated by CAT-scanning studies.

Mathematical process models will be studied to help reveal the complex interplay between the convection in the melt and the heat transfer mechanisms of radiation and conduction—all of which affect solidification.

Once interactions at the melt-solid interface are understood, a computerized feedback system will be set up to monitor data from the sensors and send corrections to a multivariable digital controller. This controller will replace the single-variable analog controller now used in the growth of GaAs crystals.

In addition, a GE-developed expert system will be linked to the sensors and to the controller. It will consider such factors as the purity of the starting materials, desired wafer properties, and crystal size.

As the crystal is growing, the expert system will monitor all sensory data for major problems. If one occurs, the expert system will assist human operators in arriving at a diagnosis and then send a corrective strategy to the controller.

JTAG boundary-scan standard

Efforts of the Joint Test Action Group are continuing toward the establishment of a standard boundary-scan testability framework for both off-the-shelf and custom ICs. JTAG's aim is to establish a standard definition of boundary-scan so that the boundary-scan chips from one vendor can be used together with those from other vendors to achieve board and system test goals.

The standard is striving for functional conformity at the device pin level rather than a detailed implementation. (For more technical discussion of the standard, see "D&T Standards" in the August 1986 issue of D&T.)

As an initial step, JTAG has produced a proposal that describes the functions and features felt to be necessary and describes how they might be used. The proposal has been distributed to JTAG members and other interested parties, including systems companies, IC and ATE vendors, and members of the academic community.

A technical subcommittee of JTAG has been established to review feedback and compare the proposal to various corresponding companies' in-house approaches that appear similar.

Copies of the proposal can be obtained from Colin Mauder, British Telecom Research Labs, Martlesham Heath, Ipswich, Suffolk IP5 7RE, UK; (44) 473-642706.

A North American working group will be formally established at its first meeting, which is planned for March/April 1987. Those interested in participating should contact Meera Pradhan, (609) 639-2262, or Rod Tulloss, (609) 639-2484. Both are located at AT&T Eng. Research Ctr., PO Box 900, Princeton, NJ 08540.

M²C to build IC facility

The Massachusetts Microelectronics Center, known as M²C, has received final approval to begin construction of an IC fabricating facility. The center, a combined effort by industry, state government, and nine public and private universities in Massachusetts, was designed to improve the level of IC design education in the state's engineering schools.

The facility will enable students to get their chips back within three to six weeks of the time the design is submitted, enabling them to test their designs under laboratory conditions in the same academic period.

Construction will start in spring 1987 with a projected completion date of early 1988.
Growth of CAEE to triple by 1990

The use of computers to engineer new electronic devices is snowballing at a rate near 30% per year in the US, according to a study by Frost & Sullivan, Computer-Aided Electronics Engineering (CAEE) in the US. Distinctions between CAD and CAE have blurred. CAE in making electronics—ICs and boards—now encompasses the entire design cycle from modeling the behavior (logic) of a system to putting out the complete specifications of a workable design. A primary reason is the advances in affordable computer technology, which have enabled a transfer from the drafting room to the engineer's desk.

The installed base of CAEE systems is expected to grow around 29% per year between now and 1990—from an estimated 58,000 seats (computers or workstation terminals) to about 151,000 by 1990. The dollar outlook is not as optimistic. Although the personal computer will be the dominant support, it will decrease from nearly half the seats sold in 1986 to little more than a third sold in 1990. The reason is that CAE applications will become more complex, making shared systems more widespread; mainframes and supermicro/minis will expand their present shares, which are slightly over a quarter each.

In market value, the report forecasts CAEE prospects in both constant and current dollars: from a base of $670 million in 1986, expected consumption in 1990 is $1.2 billion in current dollars. More than two thirds of this value is seen stemming from design tasks in PCBs, with almost one third from IC design tasks.

The computer industry is the largest CAEE purchaser, and producers of communications equipment are second. Mentor Graphics is singled out as having the largest market share in CAE, followed by Daisy Systems, Calma Co., and Computervision.

Copies of the report (#1632, 312 pp.) are available from Frost & Sullivan, 106 Fulton St., New York, NY 10038; (212) 233-1080; $1950.

Motorola undefeated in SRAM shmoo-out

In a recent contest to compare static RAM access times, Motorola emerged the winner, boasting the fastest devices in four types. A Teradyne memory tester was set up to generate shmoo-plots and to characterize the major data sheet parameters for static RAMs of 64Kx1, 16Kx4, 4Kx4, and 8Kx8. The speeds are 25, 35 ns for the first three, and 45, 55 ns for the fourth.

The advantages of using SRAMs in system design include the availability of writeable control store, I/O buffer storage, CAD/CAM/CAE, automatic test equipment, and advanced robotics with vision.

Ceramics: cost versus reliability

Ceramics may be the material of choice in future IC packaging, according to Advanced Ceramics Market Opportunities, a study by International Resource Development. Although ceramic component development has a long way to go, there is little doubt that R&D will continue to be supported, and more sophisticated products will eventually overcome the material's greatest drawback—catastrophic failure.

Qualities that attract designers are extreme hardness, low density, high melting points, high corrosion resistance, and good mechanical properties at high temperatures. Ceramic materials can also be engineered fairly easily to make them suitable in a wide range of applications.

Too expensive?

The single most limiting factor to the use of ceramics over plastics, which now occupy 70% of the market, is cost. But their flexibility and reliability may yet overcome this limitation.

Since ceramics are easily adapted to small size constraints, they will become increasingly popular as computers get smaller. Their high resistivity and low leakage tendencies help to minimize signal distortion and extraneous noise. Even more important is their ability to dissipate heat. As chips become more complex, more electrical energy is required to operate them, and more heat is given off. The amount of heat can place important constraints on circuit density and power. These qualities enable ceramic components to handle roughly double the power level of the plastic-packaged component.

Saving space

The trend to smaller, more complex computers is a boon for ceramic ICs. The large number of terminal leads required for ICs for the device interconnects necessary for advanced memory and switching circuits means that the ICs must be manufactured with advanced ceramic materials.

Leadless packaging is another development that will gain market share for advanced ceramic ICs. Instead of pins or leads on two sides of an IC package, a leadless component has solder pads on all four sides of the chip. This design reduces the space necessary to mount an IC and equalizes the conduction paths for all interconnections to the component.

Leadless chips offered commercially today include multilayer ceramic or single-layer alumina metallized technology. Using these technologies, up to 300 terminal connections are possible for a single chip.

Copies of the IRD report (#721, 221 pp.) are available from IRD, 6 Prowitt St., Norwalk, CT 06855; (203) 866-7800; $1650.