Perspectives on ITC 86

Charles Radke, IBM

"If a customer's car dies on the highway, it had better not be due to a faulty integrated circuit," said J. Wallace, president of Ford Microelectronics, pointing out the need for high-quality products in the automobile industry. Wallace was the keynote speaker at the 1986 International Test Conference held September 8-11 in Washington, DC, which addressed high quality in ICs, the need to integrate design and test, and the challenges of testing new technology.

IC quality at Ford Microelectronics has been improved from 10,000 dpm (defects per million) to 200 dpm. The reduction, Wallace believes is due to an increased emphasis on cooperation—a tight supplier and customer relationship, a common perspective on quality, and a teamwork approach. Teamwork included openness in showing test results, a common language, a commitment, and interchange of information.

"Test problems must be solved at the source," he said. Working with one supplier, Ford reduced incoming inspection from 100% to zero by using leversages such as a charge for retesting if the IC did not meet its objective.

W.D. Maris, IC director of the Elcoma Division of Philips, followed Wallace, speaking on the need to integrate design and test. In his talk, "Testability: The Achilles Heel of Design," he stressed the need to counteract the trend of high test cost. Complexity and content have increased test generation time such that today one-third of product cost is test cost.

A solution, Maris said, is to subdivide ICs into separately testable blocks (macros) that can be tested in parallel. Using the same strategy at the board level, built-in test features, such as boundary scan, can be used to divide the board into testable ICs and testable interconnections.

The use of a pure scan approach has limitations when used on modern VLSI chips containing memories, PLAs, multipliers, and ALUs, however. Also, traditional in-circuit methods of boards that reduce the problem to testing ICs can no longer be used because of the increasing use of surface-mounted devices.

The commitment of Philips to zero-defect high quality products, he said, mandated the need for a unified test strategy that can be smoothly applied at both the IC level and the board level. He cited the establishment of the Joint Test Action Group among manufacturers as the first step toward a consensus on testable design.

Richard Sedmak of Self-Test Services spoke on the topic of complex test problems associated with new technologies. Sedmak believes that traditional external testing will ultimately face permanent physical limitations, and the only solution is built-in test.

A panel took up the classical debate of the deterministic approach. Some panel members stressed the importance of knowing exactly what percentage of faults the test covers, citing the benefits of high confidence in the quality of the products. However, advocates of random testing pointed out that it is very easy to generate large numbers of random patterns and apply them at circuit speed with the aid of simple built-in test hardware.

E. McCluskey of Stanford University advocated the pseudo-exhaustive testing approach, in which logic is partitioned into blocks that can be tested exhaustively in a self-test environment. The approach eliminates the need for test generation and explicit fault modeling and simulation.

Other panel members questioned the area and performance penalties associated with the exhaustive approach, and raised the issue of failure modes that introduce sequentiality into combinational devices because these failure modes are not considered by the pseudo-exhaustive testing approach.

New test challenges in VLSI Test Workshop

W.E. Radcliffe, IBM

Current test concepts, test limitations, and future trends in microsystems were hot topics at the 1986 VLSI Test Workshop, whose theme was "Microsystems: New Test Challenges."

Opening sessions

Steve Bisset, president of Megatest, opened the workshop in a plenary session that addressed the importance of test system architecture in reducing cost of testing. He strongly suggested that development paths can be decoupled only through architectural stability. These strategic design decisions would allow successive generations of compatible software and hardware.

In "The Next 10 Years in Test Equipment," Graham Miller, president of LTX, stressed the need for high-performance test systems that can be expanded in pin count, etc. and still use the basic software. These systems should also be linkable and must be able to test devices with both analog and digital circuits.

J. Healy, president of Trilliumation, discussed issues related to "Complex Logic Testing: Today's Challenge." He indicated that three major parameters—noise, repeatability (accuracy), and capacitance— influenced acceptance/rejection criteria. Because completing a good design and testing a new product in timely fashion is critical to competing in the market, Healy recommended that design and test groups be merged.

Workshops

A total of 10 workshops addressed such topics as

1. VLSI Testing with High Speed Packages
Highlights of Workshops 1 and 2. Challenges have been created by packaging technology for VLSIs. High-speed ICs with their high pin count have necessitated greater emphasis on waveform control at IC inputs.

Optical techniques to extract signals from digital devices (both packaged and unpackaged) are quite promising because of their high speed greatly reduced loading presented to the device. Preliminary data shows signal rise times on the order of 460 fs.

Harris is performing work under contract to Rome Air Development Center to produce a detailed description of an architecture for a next generation microcircuit tester. Some of the objectives are to model a system with performance characteristics of 250-500 MHz data rates, 512 device pins, and 200-ps timing accuracy.

A major shortcoming in testing today is the absence of a link between the design engineer and the test engineer. Such a link would enable the tester to take output from the design station and convert it into test vectors automatically with a guarantee of adequate fault coverage.

Highlights of Workshops 3 and 4. Noise is just one of several factors that enter into reliability. When reliability is at a premium, weak parts should be weeded out by stress testing; testing at elevated temperatures and supply voltages. Analog measurements at the wafer test level can be used to assess noise and performance margins in MOS and BJT circuits. The Scanning Stroboscopic Electron Microscope, which is ideal for this purpose, is available for $150,000 to $300,000.

A decision-based expert system would be appropriate in the context of generating VHSIC Hardware Description Language specifications for hardware designs. A representative from Gould Research Center outlined an intelligent functional silicon compiler under development. The compiler will take behavioral specifications and design constraints and convert them into structural designs. Testability concerns would also be interpreted in this framework.

Highlights from Workshops 5 and 6. Four basic areas must be addressed when considering CAE as a vehicle for functional board test program generation. First, there is the accuracy of the simulator contained within the tool itself. Precise edge control and flexibility are prime factors to be considered. Second, is the user-friendliness of the interface tools, an issue for both the code translation and communications systems. The third consideration is tester limitations. A straightforward interface that produces test programs severely limited by ATE is of little value. Finally, the system has to support multiple simulation systems.

Representatives from IBM discussed an intelligent software system that dynamically juggles the device pins to be pulsed between comparatively few tester pulse generators during execution of the test program. Dynamic clock assignment has resolved many test problems that the company encountered during IC manufacture.

Highlights from Workshops 7-10. Automatic test generation is impractical for VLSI if “smart” is not incorporated into ATG. If ATG cannot recognize certain circuit characteristics, then processing becomes CPU intensive. A good benchmark circuit must be established to compare results of various ATG algorithms.

An inductive fault analysis procedure was described for use in predicting all the faults likely to occur in a MOS IC circuit or subcircuit. The three major steps of the procedure are (1) generate physical defects using statistical data from the fabrication process; (2) extract circuit-level faults caused by these defects; and (3) classify fault types and rank faults according to their likelihood of occurrence.

The unanimous conclusion regarding product quality was that very high stuck fault coverage (over 98%) is required for today’s VLSI chips and modules. Random patterns alone do not provide sufficient product quality. Environmental testing, such as burn-in, will continue to be a requirement. To contain, and hopefully reduce, the cost of shipping quality products, however, the boundary between design and test must continue to fade, and new test pattern generation software will have to be developed.