Strong showing at DAC 86

The 1986 Design Automation Conference, held last July, was the first major computer conference to buck the trend of reduced attendance. A grand total of 3840 paid attendees (1985 attendance was 3740) enjoyed an exceptionally strong technical program, with design productivity enhancements, improved design cycles, and emphasis in quality for design and test.

The exhibit area held 660 booths with 95 exhibitors. During the opening of the exhibits, the conference featured a new product and applications session, in which exhibitors could announce new hardware and software products to the press and attendees.

As usual, the arrangements for the technical sessions and exhibits went smoothly. The DAC is gaining a name as one of the best-run major computer conferences.

Awards

The highest level IEEE technical award, the Emanuel R. Piore Award, was given to David C. Evans and Ivan E. Sutherland for their pioneering work in the development of interactive computer graphics, which has accelerated the development of design workstations.

Best Papers. The 1986 DAC Best Paper Award in simulation and test went to S.Y. Kuo and W.K. Fuchs of the University of Illinois for their work on "Efficient Spare Allocation in Reconfigurable Arrays." The paper dealt with the problem of yield degradation because of physical failures in large memory and processor arrays. The authors recommended the use of CAD techniques to optimize reconfigurations of arrays that use spare rows and columns to improve yield.

In the high-level design category, R.H. Katz, M. Anwarrudin, and E. Chang of the University of California, Berkeley, won the award for their paper, "A Version Server for Computer-Aided Design Data." The authors discussed work on a logical organization for describing designs over time. The difficulty is to manage the complex design description as it evolves. An operational model was proposed based on workspaces and transactions. It describes how the structures can be manipulated while the sharing and integrity of the database is controlled.

Finally, in physical design, D.F. Wong and C.L. Liu of the University of Illinois were presented with a Best Paper Award for "A New Algorithm for Floorplan Design." The method proposed uses simulated annealing to produce a new representation of a floor plan that enables effective neighborhood search and a means to minimize area while achieving total interconnection length in the final solution.

Best Presentations. The Design Automation Conference also hands out awards for the best presentations. Recipients of the 1986 award were R.H. Katz (see "Best Papers") for "A Version Server for Computer-Aided Design Data"; P.G. Paulin (coauthors, J.P. Knight and E.F. Girycz) of Bell-Northern Research, Ottawa, for "HAL: A Multiparadigm Approach to Automatic Data Path Synthesis"; B. Ackland of AT&T Bell Labs (coauthor, Hiroyuki Watanabe) for "Flute: A Floorplanning Agent for Full Custom VLSI Design."

SIGDA Awards. Two meritorious service and leadership awards were presented by Chuck Shaw, chairman of ACM's Special Interest Group on Design Automation. With these awards, SIGDA, a DAC sponsor with the Computer Society of the IEEE, recognizes dedicated leadership, service, and contributions to SIGDA and its members.

The first of this year's awards went to Charles Radke (D&T's Roundtables editor) of IBM for contributions such as revitalizing SIGDA in 1970, initiating the SIGDA newsletter in 1971, serving as first chairman of the new SIGDA from 1971 to 1975, initiating SIGDA-sponsored technical sessions and workshops from 1972 to 1975, and serving on the executive committee of the Design Automation Conference from 1978 to 1986.


David Evans (right) and Ivan Sutherland receive IEEE's highest award, The Emanuel R. Piore Award, for their work in interactive computer graphics, a significant development for design workstations.

Charles Radke (left) of IBM receives SIGDA achievement award from Chairman Charles Shaw.
Scholarships

One or more scholarships of $8000 are given each year by ACM SIGDA and the IEEE Design Automation Technical Committee. Awards are presented to graduate engineering and computer science schools based on proposals submitted to SIGDA and DATC. Awards are made to a university, which can, among other things, select one or more students for support. The dean or other school representatives receive the awards at the DAC. This year there were two recipients. For Portland State University in Oregon, Dr. Marek Perkowski of the Electrical Engineering Dept. accepted the award as a scholarship in the name of David Smith. For Purdue University in West Lafayette, Indiana, Prof. Samuel Stevens of the Electrical Engineering Dept. accepted the grant award.

Those interested in applying for this grant award should contact Lawrence O'Neill, AT&T Bell Labs, 2B-327, Crawfords Corner Rd., Holmdel, NJ 07733.

Keynote speech

The Design Automation Conference keynote speech was given by Robert M. Williams who is responsible for computer-integrated manufacturing within IBM. As assistant group executive of the Information Systems and Communications Group and general manager of Industry Systems Products, he was well-qualified to speak on the “IBM Perspective on the Electrical Design Automation Industry.”

Williams stressed that the DA community often loses sight of the overall impact of design automation because of members’ everyday involvement. He called this period both “The Electronic Age” and “The Age of Design Automation” because design automation has provided the fundamentals of much of today’s progress.

In his keynote, Williams reviewed three decades of IBM use and development of DA. He described IBM’s approach to providing software and hardware to the DA industry and commented on what he sees in the future.

He concluded his history of IBM by saying that at present, 5000 IBM designers in 27 research and development sites in seven countries use DA systems. Products range from single-chip products to the complex 3990 mainframe. IBM’s extensive use of DA was demonstrated by the fact that approximately one large mainframe is assigned for DA per 100 designers. He indicated that within IBM the demand is growing about 30% each year within IBM.

The core of design support is provided by IBM’s Engineering Design System organization, which provides the system framework for designing and developing IBM products. EDS represents significant resources. There are nearly 10 million lines of source code, excluding such items as technology rules and catalog procedures. Each year over 1000 different printed circuit boards and 2000 unique chips are designed and released, representing around 20 million circuits. Williams emphasized that four years ago the same number of designers designed one-fifth that number of circuits, and in those four years the design EC (engineering change) cycles have gone from five to two, or in some cases to a single pass. Today, IBM has a ratio of one DA developer or support person for every six designers.

Williams indicated that IBM’s approach to the multifaceted, multivendor electrical market is to provide a consistent environment having an open architecture with hardware, operating systems, and a family of DA applications as complete as possible. The hardware platform accepted was the PC XT, the PC RT, and the System 370. He said that since IBM could not possibly produce all applications program requirements, DA vendors were encouraged to provide products on any or all of IBM hardware. The aim is for consistent operating systems, language support, and communications for both workstations and mainframes. IBM was committed to interfacing to industry communication standards such as the recently announced Ethernet support and the IBM Token Ring support on the PC RT. He stated that last January the CIEDS (Computer-Integrated Electrical Design Series) were announced.

Williams concluded by looking into the future, after the obviously automatable has been automated. The future will bring more complex and challenging tasks: automating the creative part and producing consistently good designs on the first pass. He saw three key challenges:

1. Design integrity, including the integration of data from various design systems and functions,
2. Response to a competitive environment, where products will need to move to significantly higher levels of quality (led, no; by the Japanese, but by the economic impact of low-quality products),
3. Design support, including the description and distribution of technological information.

Support for application-specific integrated circuits will be a key area. Although less than 10% of all designers produce ASIC chips, in the future more than 60% of designers will require ASIC design support.
FTCS-16: A touch of old Vienna

Sharad C. Seth  University of Nebraska

The 16th International Symposium on Fault-Tolerant Computing, held in Vienna, Austria, opened to the pleasing sound of woodwind music performed by a local group. During the ceremony in the Auditorium Maximum of the Wirtschaftsuniversitat (Economic University) of Vienna, Dr. W.C. Carter of IBM was recognized for his long and significant contributions to fault-tolerant computing and service to the symposium.

Afterwards, the conference began its traditional format of two parallel sessions. The talks in these sessions were not well synchronized, making it difficult to "session hop," so this report describes sessions selected according to my own interests.

Altogether, 63 papers were presented (out of the 292 submitted) in 20 sessions. The authors came from 22 countries, making this FTCS truly an international gathering.

Design for testability

M. Nicolaidis and B. Courtois proposed NMOS designs that allow concurrent error detection of unidirectional errors, using error-directing codes. Their main contribution was the use of a lower level fault hypothesis in which technology-dependent faults, such as transistor ons and opens, were considered.

A BIST scheme for a CMOS ALU was described in the paper by E. Cerny, G. Bois, and M. Abouhamid. This scheme uses dynamic logic and is based on the ρI concept (partitioned I) testability of one-dimensional, unilateral, iterative logic arrays. All functional faults (and some others) are detectable by a number of tests that are independent of the number of bits in the ALU.

K.E. Grosspietsch, H. Huber, and A. Muller demonstrated a model of a fault-tolerant and easily testable associative memory. K.K. Saluja and R. Kandapani proposed a BIST design method for sequential circuits based on checking experiments. This design adds a controllable input and rearranges the states of a given state table. The proposed modification can be carried out after the circuit has been designed, but the applicability of the method appears to be limited to small machines.

S.C. Seth, B.B. Bhattacharya, and V.D. Agrawal described an extension of their Predict testability analysis method presented at last year's symposium. The extension overcomes inaccuracies in the computation of line observabilities.

Arithmetic functions implemented in hardware can often be expressed by recurrence relations. This year D. Bhattacharya and J.P. Hayes extended earlier work by Abraham and Gajski by explicitly introducing a small number of control inputs to facilitate testing. They demonstrated that the area-time complexity of such modifications is quite attractive.

A. Avizienis, a founder of the symposium and a pioneer in computer arithmetic, presented a two-dimensional generalization of the low-cost residue codes. He illustrated by examples his algorithms for byte serial checking, complementing, and addition operations for operands encoded in the two-dimensional residue codes.

Testing

Of the six papers in the two testing sessions, two dealt with random testing and the rest with deterministic testing. In the latter group the most interesting was the paper by Y. Levendel and P.R. Menon on input transition test generation and fault simulation. Such tests detect faults that change the timing of certain transitions, such as the open-transistor faults in CMOS circuits.

V. Pitchumani and S. Soman presented an approach to test generation in which only the function of a circuit needs to be known. Using the divide-and-conquer metaphor, they split the function into two or more unate components, recursively computed a good functional test set for each, and combined the solution. When compared with random tests of the same size, this method covered more faults.

N. Itazaki and K. Kinoshita extended the test-generation algorithm Podim to circuits with tristate modules. In another paper, Cheng and Patel used divide-and-conquer to generate tests for one- and two-dimensional ILAs for both single- and multiple-cell faults.

The paper by A. Fuentes, R. David, and B. Courtois analyzed the question of random vs. deterministic testing of RAMs in terms of test length. Their surprising conclusion was that random test length remains linear over a variety of fault models, while the deterministic test length can become $O(n \log n)$ for some types of faults. However, the constants of proportionality are much higher for the random test lengths, casting doubts on its eventual benefits.

Built-in Self Test

A. Hlaviczka suggested a parallel multisignature analysis of a multiple output circuit under test and showed how it could be used to test a basic microcomputer structure consisting of a processor and a ROM. The key idea of their $k$-signature parallel analysis (kSPA) is to form $k$ different signatures of the same stream, where each signature uses the MISR with a different feedback.

P. Golan, O. Novak, and J. Hlavicka proposed a test pattern generation scheme well suited for circuits designed with the structured design method called random access scan. Unlike LSSD, RAS assumes that each latch in the circuit under test can be accessed randomly by its assigned address. The authors' scheme uses two linear feedback shift registers (LFSRs), one to generate a scan address and the other to generate a test pattern to be scanned into the address. They show simulation results in support of their claim that the proposed scheme gives better results than random testing.

Y. Zorian and V.K. Agrawal questioned the simplified assumption made in the analysis showing low error-masking probability of MISR schemes; namely, that error patterns are uniformly distributed. In an elegant generalization of their earlier work, they showed how output data could be modified at a reasonable cost to reduce the error-making probability in a BIST environment.

In the final paper of this session, W.C. Carter showed a way to construct parallel signature analyzers that can detect one, two, three, or any odd number of errors.
Conclusion

There were several strong papers at the conference, but the sessions were not always carefully put together and often lacked coherence. Nonetheless the symposium overall must be considered a great success. The organizers are to be congratulated for a good job in getting a very large number of submissions of papers from many parts of the world, and for enforcing rigorous and fair standards in the paper review process. They also augmented the technical program with two outstanding social events: the reception by the Mayor of Vienna on the second day and the visit to the Heiligenkreuz monastery on the third day, followed by a Heurigen party at Gumpoldskirchen.

ICCAD-86: A New Home and Burgeoning Interest

The International Conference on Computer-Aided Design, a conference targeted for EE CAD professionals, has come a long way in its four-year history. ICCAD-86, which will be held November 10-13, 1986, promises to be the most successful one yet. A greater-than-ever number of internationally recognized CAD experts have responded to the ICCAD Calls for Papers. The conference also has a brand new home—the Santa Clara Convention Center in California.

Indeed, many CAD professionals and users now consider the conference one of the premiere forums for learning about leading-edge developments in computer-aided design.

Technical sessions

The 116 papers in ICCAD-86 were selected from over 325 proposals, thereby ensuring that only the very best are included in the expanded technical program. As in the past, the technical program will emphasize CAD for integrated circuit design and electronic system design. All told, 36 technical sessions will be held over the three days.

The technical sessions fall into four broad categories: systems, simulation, test, and layout, including such topics as

Systems. CAD tool integration, synthesis from a behavioral description, rule-based synthesis, finite-state-machine and data path synthesis, control logic synthesis, verification of logic correctness, multilevel verification, multilevel logic minimization and optimization, logic minimization using simulated annealing, hardware acceleration of circuit and fault simulation, and functional verification of MOS circuits.

Simulation. Waveform relaxation techniques, statistical and functional timing analysis, simulation on multiprocessors, statistical modeling of ICs, yield simulation, modeling VLSI interconnection, process simulation on a supercomputer, two- and three-dimensional modeling techniques, and CAD for process design.

Test. Testing microprocessors, built-in self-test techniques, logical design rule checking, design-for-testability, new developments in automatic test pattern generation, testing bit-serial logic and wafer-scale arrays, and multilevel fault simulation.

Layout. Power and ground routing, placement speedup using hardware accelerators, module generation and layout synthesis, gridless routing, global routing techniques, new techniques in gate-matrix layout, simulated annealing, new theoretical approaches to placement, placement and routing for wafer-scale integration, and symbolic layout and compaction.

Two timely and intriguing panel sessions will highlight the activities on Tuesday evening, November 11. In "Is There a Future in Parallel Processing for CAD Applications?" a panel of experts will try to sort out promise from reality. In "Which Operating System Will Win for CAD?" proponents of the most popular operating system—Unix—will square off against those who support a different solution.

Banquet speaker

Traditionally, the conference banquet dinner features a thought-provoking and entertaining speaker, and ICCAD-86 carries on this tradition. Dr. Tom Paine, a former director of NASA and recently chairman of the National Commission on Space, will describe the process of "Pioneering the Space Frontier."

Tutorials/Workshops

On November 10, ICCAD-86 will sponsor four all-day tutorials and one workshop. The tutorials are "Silicon Compilation," "VLSI Layout," "Design-for-Testability," and "Information Management for Engineering Design."

The conference will also host a workshop on EDIF—the Electronic Design Interchange Format. This year, tutorial/workshop attendees will be required to register for the conference. If the tutorial sessions at previous conferences are a guide, these sessions at ICCAD-86 are likely to be very popular. Advance registration (the registration form is on p. 00 of this issue) is strongly advised both to ensure attendance and to reduce cost to the attendee.

How to attend

For conference or registration information, contact MP Associates, 7366 Old Mill Trail, Suite 101, Boulder, CO 80301; (303) 530-4562. For travel arrangements and assistance, call Mission Park Travel at (408) 980-1000. Room reservations must be made directly with the conference hotels: Doubletree Hotel, (800) 986-0700, or Santa Clara Marriott, (408) 988-1500. Room reservations made after October 26, 1986, will be subject to availability.