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Conferences sponsored or cosponsored by
the Computer Society of the IEEE are so in-
dicated by the society's logo. To list a conference
in Calendar, submit the information at least
six weeks before the month of the issue it will
be published in. This magazine is published in
February, April, June, October, and Decem-
ber. Send the listings to IEEE Design & Test,
Calendar, 10662 Los Vaqueros Circle, Los
Alamitos, CA 90720.

October 1986

Workshop on Design Principles for Experimental Distributed Systems, October 16-17,
West Lafayette, Ind. Contact Samuel Conte,
Dept. of CS, CS Bldg., Purdue Univ., West
Lafayette, IN 47907; (317) 494-6005.

SPIE Symp. on Advances in Intelligent Robotics Systems, October 26-31, Cambridge,
Mass. Contact SPIE Tech. Prog. Committee,
1986 Cambridge Symp., PO Box 10, Belling-
ham, WA 98227; (206) 676-3290.

IEEE Galium Arsenide IC Symp., October 28-30, Grenelefe, Fla. Contact Robert Mar-
kunas, Research Triangle Inst., PO Box 12194, Research Triangle Park, NC 27709;
(919) 541-6153.

November 1986

Automated Manufacturing Exhibit and Conf., November 3-6, Greenville, S.C. Contact AM-
86, PO Box 5616, Greenville, SC 29606; (803) 239-2967.

Int'l Workshop on Symbolic Layout and Compa-
 nation, November 5-6, Chapel Hill, N.C.
Contact Franc Brglez, MCNC/BNR, PO Box
12889, 3021 Cornwallis Rd., Research Tri-
angle Park, NC 27709; (919) 248-1800.

ASSP Workshop on VLSI Signal Processing,
November 5-7, Los Angeles. Contact S.Y.
Kung, Image Processing Inst., Powell Hall,
Univ. South. Calif., Univ. Park, Los Ange-
es, CA 90007; (213) 743-6581.

Applied Robotics and Design Automation
Conference, November 10-12, St. Louis, Mo.
Contact A.H. Soni, Sch. Mech. and Aero-
space Engineering, Oklahoma State Univ.,
Stillwater, OK 74078; (405) 624-5900.

Int'l Conf. on Computer-Aided Design,
November 10-13, Santa Clara, Calif.
Contact MP Assoc., 7366 Old Mill Tr., Suite
101, Boulder, CO 80301; (303) 430-4562.

Autofact Conf. and Expo, November 11-14,
Detroit. Contact SME, One SME Dr., PO Box
930, Dearborn, MI 48121; (313) 271-0023.

Fifth VLSI Packaging Workshop, November
17-18, Paris. Contact Karel Kurzweil, Bull-
Rue Jean Jaures, 78340 Les Clayses Sous Bois,
France; (33) 13-462-7048.

December 1986

Electrical and Electronics Conf. and Expo.,
December 1-3, Toronto. Contact IEEE Cana-
dian Regional Office, 7061 Yonge St., Thorn-
hill, Ontario L3T 2A6, Canada; (416) 881-1930.

Int'l Computer Symp., December 15, Tainan,
Taiwan. Contact Ming T. Liu, Dept. of Com-
puter and Information Science, Ohio State
Univ., 2036 Neil Ave., Columbus, OH 43210;
(614) 422-1837.

January 1987

SCS Multiconference, January 14-16, San
Diego. Contact Soc. for Computer Simula-
tion, PO Box 17900, San Diego, CA 92117;
(619) 277-3888.

Second Topical Meeting on Picoscend Elec-
tronics and Optoelectronics, January 14-16,
Incline Village, Nev. Contact Optical Soc. of
Am., Picoscend Elec. and Optoelec., 1816
Jefferson Pl. NW, Washington, DC 20036.

Design Automation Workshop, January
20-23, Apache Juncton, Ariz. Contact
James Armstrong, Dept. of EE, Virginia Tech,
Blacksburg, VA 24061; (703) 961-7078.

Fourth Int'l Symp. on Modeling and Simu-
lation Methodology: Intelligent Environ-
ments, Goal-Directed Models, January 21-23,
Tucson, Ariz. Contact Bernard Zeigler, ECE
Dept., Univ. of Ariz., Tucson, AZ 85712;
(602) 621-2108.

February 1987

Third Int'l Conf. on Data Engineering, February 2-6, Los Angeles. Contact
IEEE Computer Society, 1730 Massachusetts
Ave. NW, Washington, DC 20036; (202)
371-0101.

Systems Design and Integration Conf., Febru-
ary 10-12, San Francisco. Contact Deanna
Myerson, Elec. Conv. Mngmt., 8110 Airport
Blvd., Los Angeles, CA 90045; (800) 421-0816
or (800) 262-4208 (in Calif.)

Third Conf. on Artificial Intelligence
Applications, February 22-28, Orlando,
Fla. Contact Jan Aikins, Aion Corp., 101
Univ. Ave., Palo Alto, CA 94301; (415)
328-9595.

IEEE Int'l Solid-State Circuits Conf., Feb-
uary 25-27, New York. Contact IEEE, 345 E.
47th St., New York, NY 10017; (212) 705-7900.

Sixth IEEE Phoenix Conf. on Com-
puters and Communications, February
25-27, Scottsdale, Ariz. Contact Forouzan
Golshani, Dept. of CS, Ariz. State Univ.,
Tempe, AZ 85287; (602) 965-2855.

Int'l Solid-State Circuits Conf., February
25-27, New York. Contact IEEE, 345 E. 47th
St., New York, NY 10017; (212) 705-7900.
March 1987

VLSI Test Workshop, March 24-25, Atlantic City, N.J. Contact Wesley Radcliff, IBM, E. Fishkill Blvd., Bldg. 321-SEI, Dept. 277, Howell Junction, NY 12533; (914) 894-4346.

Second Int'l Conf. on Robotics and Factories of the Future, March 24-27, Salt Lake City, Utah. Contact R. Radharaman, Dept. of Mechanical and Indus. Engrg., College of Engrg., Univ. of Utah, Salt Lake City, UT 84112; (801) 581-2241.

IEEE Int'l Conf. on Robotics and Automation, March 30-April 2, Raleigh, N.C. Contact Harry Hayman, 738 Whitaker Terr., Silver Spring, MD 20901; (301) 434-1990.

April 1987

Fourth Int'l Workshop on Software Specification and Design, April 3-4, Monterey, Calif. Contact M.T. Harandi, Dept. of CS, Univ. of Ill. at Champaign-Urbana, 1304 W. Springfield, Urbana, IL 61801; (217) 333-4666.

Second Tech. Workshop: New Directions for IC Testing, April 8-10, Winnipeg, Canada. Contact D.M. Miller, Dept. of CS, Univ. of Manitoba, Winnipeg, MB R3T 2N2; (204) 261-4528.

IEEE Microelectronics Conf. and Exhibition (Miconex 87), April 21-23, Winnipeg, Canada. Contact E. Gonzalez, Infotech Manitoba, 1970 Ness Ave., Winnipeg, Canada R3J 0Y9; (204) 896-2222.

D&T ROUNDTABLE

Continued from page 67

Agrawal: I hope that as you are trying to make correct circuits, you will also make testable ones, which means you will include design for testability in your synthesis.

Karasu: I think redundancy in a combinatorial circuit depends mainly on the variety of behavioral level input and the logical primitives that you can use in the synthesis system. We can eliminate redundancies through optimization. We can add scan-in, scan-out features in each register to make it testable.

D&T: I imagine for a moment that you are the Ann Landers of logic design. What advice would you give designers? What should they watch out for?

Karasu: Over 20 years ago, the automatic camera with an automatic exposing system was introduced. At the time many professional cameramen said it would be of no use because photography required experience that cannot be built into a camera. Nowadays anyone can use a camera with automated features because we learned how to use the technology. I think logic synthesis is similar. Today's designers have no experience with logic synthesis features. When they start to use the synthesis programs, they will develop their own techniques. After all, they are the ones who will be doing the designs. They will learn how to make the best use of logic synthesis.

Brayton: My advice is the techniques are here, they work, and if you see your CAD support people not moving toward a logic synthesis system, get on them and say, "This is the way of the future. Let's get with it."

Gregory: My advice is along the same lines. The Design Automation Conference clearly shows that logic synthesis is here. We can synthesize circuits from Boolean equations that are as small and as fast as those optimized by hand.

Joyner: I think designers have to begin using a synthesis tool. They'll see its benefits, that it allows them to concentrate on doing the initial design and supplies them with other needed data, such as timing information. But they have to use the tool.

Pursuing the analogy of the automatic camera, the camera's evolving features have made it appropriate to a wider range of applications. This will also happen with logic synthesis, although manual design will continue to play a role. Logic design will not meet 100% of all design needs, but it will address an increasing proportion of them.

D&T: I thank all of you for your participation. I certainly learned from this discussion, and I think our readers will also.