Paving the way for testability standards

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The efforts of an international group, called Joint Test Action Group, may determine the future of testability standards in hybrid and PCB products created by the combination of complex ICs and surface-mount technology. The companies involved in JTAG are keenly aware of the extreme difficulty of using traditional techniques such as in-circuit testing for testing surface-mount products. The group feels that these problems will eventually become evident throughout the digital electronics industry, and can be solved only through the collaboration of IC users and those responsible for chip design.

JTAG was established as a result of an initiative within Philips. Its members include representatives from:

- AT&T (USA)
- British Telecom (UK)
- Bull Systemes (France)
- Electronik Centralen (Denmark)
- GEC (UK)
- ITT (Europe)
- Marconi (UK)
- Philips (The Netherlands)
- Plessey (UK)
- Siemens (West Germany)

The group hopes to solve the testing problems that have resulted from an increase both in the number of IC packages used on a product and in the complexity of the IC itself.

The problem. Automated equipment for testing electronic products is coping with these increased complexities, but its cost is also rising. The price of fewer defects in shipped products is high when surface-mount technology is involved. Today's manufacturers of assembled PCBs typically use both in-circuit and functional board test systems, either separately or in sequence, both of which are trouble with surface-mount technology—particularly when components are densely packed. For example, the cost of bed-of-nails test fixtures for surface-mount technology is high and, when components are densely packed, probing can be impossible. Clearly then existing test technology will face increasing difficulties as surface-mount technology continues to develop. The way forward seems to be to use structured design techniques at the board level, rather than to evolve existing test strategies.

A possible solution. Boundary-scan (see box below) is a design structure that can be included in IC design to solve problems in testing assembled surface-mount digital circuits. In boundary-scan, a shift-register latch is placed adjacent to each component pin so that signals between chips can be controlled and observed using scan testing methods. The figure below illustrates.

If the technique is applied in all the ICs used to produce a product, the resulting boundary-scan path can be used to test for most defects introduced by the assembly process, such as open-circuits, solder-splashes, and wrongly inserted or incorrect components. In effect, the boundary-scan-path test can detect many of the faults that in-circuit testers are supposed to detect, but without the need for extensive bed-of-nails access or expensive test equipment.

In addition, Bull Systems and other JTAG organizations have successfully applied the technique where custom devices are used throughout a product's design. True, the full benefits of boundary-scan are gained when all components used to build a product include a boundary-scan path (including merchant parts such as microprocessors and other complex functions). However, there are also considerable benefits when only some of the components have the facility. For example, the ability to control and observe internal circuit connections improves with even an incomplete boundary-scan path, since it enables the partitioning of the assembled design into smaller, more easily tested blocks.

What JTAG is doing. JTAG's objective is to produce a functional definition for a boundary-scan architecture that is acceptable to its member organizations, and to promote this architecture as a standard. The description will give organizations as much freedom as possible to develop a detailed design of the boundary-scan path within ICs; the description's primary goal is to ensure that ICs with differing implementations can be used together in the desired manner.

A major part of JTAG's activities will be to promote the use of boundary-scan architecture in merchant ICs. Several major IC vendors have already been contacted, and JTAG hopes to continue its discussions during the coming months.

What can you do? To find out more about JTAG and its objectives, or to add your support, please contact the following JTAG members:

- Rod Tulloss, AT&T Engrg. Research Ct., PO Box 900, Princeton, NJ 08540; (609) 639-2484; or Harry Bleeker, Philips Telecomm. and Data Systems, PO Box 32, 1200 JD Hilversum, The Netherlands; (31) 35-891377.

Boundary-scan technology

The figure below illustrates the use of the boundary-scan architecture within a product assembled from several ICs. Here, boundary-scan paths for individual ICs are connected to form a single path through the complete design. They could also have been connected to form several shorter scan paths.

The figure shows that connections into and out of ICs are made through boundary-scan cells, and one possible implementation for such a cell is illustrated. Note that, depending on the control signal applied to the multiplexer, data is either loaded into the scan register from the input port, or driven from the register through the output port. The design of the cells is similar for both input and output connections of the IC. Connections between ICs can be tested by shifting values into the cells associated with IC output connections, performing a parallel-load operation, and shifting the results now stored in the cells associated with IC input connections out of the circuit for inspection. If the ICs' internal design permits, the boundary-scan path can be used in a similar way to test the circuitry within the ICs.