1986 PROGRAM OVERVIEW

The 1986 technical program continues the tradition which has made ITC the world's leading forum for technical communication between test professionals. This year's theme, "Testing's Impact on Design and Technology", is reflected by focus on the impact to device implementation by built-in self test, on design for testability, and by the addition of a new topic area to the ITC program: the interaction of CAE/workstation technology and the test engineer.

Some other highlights of ITC 1986 are:

- A panel on advanced burn-in and life-test techniques. This will be of special interest to engineers concerned with high field reliability especially for military and aerospace applications.
- Panel discussions of other hot topics, such as ISDN devices, the economics of ATE selection, and hardware modeling for test simulation.
- Presentations on testing of ultra high-speed devices.
- A special session on inexpensive, but effective, test methods.
- Expansion of the very popular topic area of artificial intelligence applications to test technology.
- Late breaking developments in the area of test generation and test software.

I believe you will agree that 1986 ITC has an exceptionally strong and wide ranging technical program. I'll look forward to seeing you there!

Pete Bottorff
1986 Program Chairman

MONDAY, PLENARY SESSION

September 8, 9:00 a.m.-12 noon
KEYNOTE ADDRESS and INVITED SPEAKERS

KEYNOTE SPEAKER:
John R. Wallace, President — Ford Microelectronics, Inc., Colorado Springs, Colorado

"Look Who's Refueling the Technology Race"

SUMMARY: Ford Microelectronics has a unique perspective on the challenges facing the test industry from its vantage point as an entrepreneurial division of the Ford Motor Company. Competition for improved quality in the automotive world has caused Ford and others to challenge standard design and test methodology. Although we have often looked in the past to small start-up companies for breakthrough ideas and innovations, we are beginning to see more examples of large, mature corporations advancing electronics technology, particularly in areas such as testing and reliability, which are so critical to a company's reputation as a quality supplier.

Just five years ago, who would have predicted Ford Motor Company to have such an expertise within the integrated circuit industry, or General Motors within data processing? By acquiring or developing these centers of technology, large corporations can take advantage of the combined strengths of small and large companies — the ability to react quickly to changing market conditions, and the power and resources to encourage and create technological innovation.

This address will discuss what's ahead for the test industry based on the innovations and new directions of companies such as Ford.

INVITED SPEAKERS

W. D. Maris, Director — Elcoma Division Philips, Eindhoven, The Netherlands

"Testability, the Achilles Heel of Design"

SUMMARY: Product quality is an important aspect of marketing. The performance indicators for the quality of a complex system composed of many integrated circuits are not only lifetime and reliability, but certainly also zero defects. Only with appropriate test strategies can the latter be achieved.

Testability is becoming the Achilles heel threatening the zero-defect goal. A number of activities has been initiated to produce a consistent and uniform test strategy in which the various aspects of IC and board testing are smoothly coupled. Based on the principles of scan-test, the design is partitioned into testable modules. For this partitioning, the IC and board design engineers are provided with a set of testability design rules.

For a full integration of a systematic test methodology into PC boards, testability has been brought to the attention of IC manufacturers. The establishment of JETAG, the Joint European Test Action Group, is a first step towards a consensus on testable design.

Richard M. Sedmak, President — Self-Test Services, Ambler, Pennsylvania

"On the Possible Limits of External Testing"

SUMMARY: Traditional testing, which is based on the generation and application of tests by external means,

suffers from a number of inherent weaknesses which threaten to limit its continued practicality in the future. These shortcomings are rooted in the constrained accessibility of internal circuit nodes from input/output pins, and hence from the tester. Unfortunately, as breakthroughs in semiconductor technology spawn faster and denser integrated circuits, these inherent weaknesses are yielding dramatically rising testing costs, or in some cases, deteriorating product quality.

The presentation begins with a discussion of the impact of circuit and packaging technology on the generation and application of tests by external means. Trends in these technological areas, as well as some results achieved by the author and others on cost/performance modeling of the conventional testing process, are used as a basis for asserting the existence of, and hypothesizing the nature of, the possible limits of external testing.

Michael J. Roberts, Director of Product and Test Engineering — GigaBit Logic, Newbury Park, California

"Challenges in AC Testability — Testing Gigahertz Logic"

SUMMARY: Gallium arsenide digital integrated circuits present new and very challenging problems to the test engineer. The inherently superior speed performance of GaAs ICs, compared with silicon devices, along with their current low level of application and use in test equipment, result in readily outrunning the performance of test systems. The performance realm in which GaAs ICs operate is one in which wiring resembles plumbing, logic signals look sinusoidal, and distance is time.

This paper identifies some of the fundamental problems, describes possible solutions, and poses future challenges in this area of IC testing.

Arthur Braun, Vice President — General DataComm, Inc., Middlebury, Connecticut

"Testing VLSI Devices for Telecommunications Products"

INTERNATIONAL TEST CONFERENCE

MONDAY

September 8, 1:30 p.m.-5:00 p.m.

MONDAY, SESSION 1

September 8, 1:30 p.m.-5:00 p.m.

DESIGN TECHNIQUES FOR BUILT-IN SELF-TEST
J. Savir — IBM Corporation (Chairperson)
R. Sedmak — Self-Test Services (Organizer)

SUMMARY: The first of two sessions on built-in self-test, this session focuses on BIST design techniques for combinational circuits, sequential circuits, and RAMs.

MONDAY, SESSION 2

September 8, 1:30 p.m.-4:30 p.m.

USING TEST DATA FOR PROCESS IMPROVEMENT
R. J. Faubert — GenRad Inc. (Chairperson)
R. J. Faubert — GenRad Inc. (Organizer)

SUMMARY: Measurements and feedback on process problems is vital to improvements of product quality. This session presents a variety of useful techniques for process data collection and analysis.

MONDAY, SESSION 3

September 8, 1:30 p.m.-5:00 p.m.

TEST GENERATION APPROACHES AND ALGORITHMS
J. P. Barlow — IBM Corporation (Chairperson)
J. P. Barlow — IBM Corporation (Organizer)

SUMMARY: As test generation strategies and systems have evolved, so have the problems they have had to address. The papers in this session describe work which has been done to solve today's test generation problems.

MONDAY, SESSION 4

September 8, 1:30 p.m.-5:00 p.m.

MEETING THE PERFORMANCE AND COMPLEXITY CHALLENGE OF VLSI
P. Brothers — Fairchild (Chairperson)
K. Mandl — Sperry Corp. (Coordinator)

SUMMARY: This session looks at test and testability concerns arising from the growing complexity and performance of VLSI.

MONDAY, SESSION 5

September 8, 1:30 p.m.-5:00 p.m.

TRENDS AND TRADEOFFS IN TEST ECONOMICS
D. Nelson — UTMC (Chairperson)
C. Weller — GenRad STG (Coordinator)

SUMMARY: This session covers 1) ASIC Verification: Where we're at and where we're going. 2) Memory chips: test cost vs. quality level. 3) Tester reliability. Closing: a panel discussion on the economics of choosing ATE.