The theme of the 1985 International Test Conference was "The Future of Test." It was chosen not only because of the nature of many of the papers presented, but also because in a very real sense this theme has always been present in the conference. The International Test Conference Committee has always strived to present a program that provides a mix between papers that address today's test problems and those that advance the frontiers of test technology.

The success of this approach—addressing the present while looking toward the future—can be judged by the growth of the International Test Conference. At its inception in 1970 as a Memory Test Symposium, it was held at a small Cherry Hill, New Jersey, inn. The 1985 International Test Conference in Philadelphia was hosted by two hotels simultaneously.

In 1985 a formal session on artificial intelligence applications to test was added to the conference. I am pleased to report that attendance at the session was extremely good and that it will become a permanent addition to the program.

Building on the success of our approach, we also added a session on probing and test fixtures; this too was well received. With the ever-increasing performance capabilities of devices and printed circuit boards, maintaining signal integrity between the test system and the unit under test poses a real challenge to test engineers and the test industry at large.

This month's issue of IEEE Design & Test features five articles that have been expanded since their presentation as papers at the 1985 International Test Conference. They were selected to provide a sampling of the subjects dealt with at the conference. Of course, five articles cannot totally represent the more than 20 subject categories covered at ITC.

As memory storage capacities continue to increase, the test time—and therefore the cost of memory devices—increase as well. Since typical test algorithms require the memory locations to be accessed many times during the test (on the order of \( N^{1.5} \), where \( N \) is the number of cells), test costs can easily dominate the total cost of large semiconductor RAMs. T. Sridhar of Texas Instruments offers an approach using parallel signature analyzers that can re-
duce test times by several orders of magnitude while requiring very little additional area on the chip.

Debugging LSI/VLSI designs quite often requires probing the internal device nodes. This is usually accomplished using miniaturized mechanical probes. More recently, some companies have started using scanning electron microscopes to perform “contactless” electron-beam probing of the internal nodes. T. Tamama and N. Kuji of the NTT Atsugi Electrical Communication Laboratory describe the system developed by NTT. Its uniqueness stems from the marriage of the electron microscope to the CAD database.

Performing ac parametric tests on high-performance devices and obtaining measurement correlation with a bench “standard” fixture is difficult at best. D. Petrich of Micro Component Technology develops a technique using simple models and Spice simulation to generate correlation parameters, which can be used to achieve correlation with the bench fixture in lieu of “golden devices.”

M. Abramovici, J. J. Kulikowski, P. R. Menon, and D. T. Miller of AT&T Information Systems present an article on LAMP2, a design aid system used within AT&T to support the design of VLSI circuits and systems. LAMP2 is a descendant of LAMP and incorporates new concepts and algorithms used to generate tests for large electronic circuits.

C. F. Hawkins of the University of New Mexico and Sandia National Laboratory, and J. M. Soden, also of Sandia National Laboratory, discuss the inadequacy of stuck-at models in dealing with gate oxide shorts in CMOS ICs. Ample experimental data and results are presented to show the effects of gate oxide shorts in different gate regions. The authors show the benefits of testing for excessive $I_{DD}$ currents to catch this failure mode. This paper received the Best Paper Award for the 1985 International Test Conference.

I am pleased to have been able to bring these articles together for this special issue, and I look forward to seeing many IEEE Design & Test readers at ITC 86.

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First Call for Participation

Annual IEEE Design Automation Workshop

Sponsored by
the IEEE Design Automation Technical Committee

Purpose of the Workshop
The purpose of this year’s Design Automation Workshop is to assess the role of artificial intelligence in the design automation process. Specifically the workshop will have sessions on:

1. The Fundamentals of Logic Based Programming - essentially a tutorial on the logic based programming techniques as employed in such languages as PROLOG and LISP.
   
2. Critique of Existing AI Systems - the strong and weak points of existing AI systems will be discussed. Most of the systems discussed here will be in the digital design area but other examples may be drawn from other fields if the experience there seems relevant.
   
3. New Potential Application Areas for AI - here the discussion will center on defining a list of important problems in the CAD area which could benefit from the application of artificial intelligence techniques.
   
4. New Advances in Artificial Intelligence and Related Support Fields - in this area discussion will center on new trends in artificial intelligence and their potential impact on CAD. One area of particular interest here is the emergence of computer architectures specifically designed to interpret rule based programs, e.g. the Japanese 5th Generation Machines.

Workshop Location
Gold Canyon Ranch is located in the scenic Superstition Mountains, 25 miles east of Phoenix, Arizona. The location thus provides a relatively secluded location for the workshop yet is conveniently located close to a major airport. Recreation activities include horse back riding, hiking, swimming, golf, and tennis. The elevation of the ranch is 1715 feet. The climate is very sunny and warm and the humidity very low.

Participation in the Workshop
Attendance at the workshop is limited to 55 persons. To participate in the workshop, please submit a short summary of your interests and activities. If you would like to make a presentation at the workshop also submit a short summary of your proposed talk. Send this information to the workshop chairman, Jim Armstrong. If you have any suggestions for session themes or would like to organize a session contact Gary Leiva, the program chairman.

More Information
If you wish more information about the workshop, contact the workshop chairman. Also, as the time for the workshop draws nearer, you will receive a detailed program for the workshop as well as information on registration at and access to the Gold Canyon Ranch.