Las Vegas to host 23rd ACM/IEEE Design Automation Conference

The 23rd ACM/IEEE Design Automation Conference will be held June 29-July 2, 1986, in Las Vegas, Nevada. An estimated 4000 attendees are expected when the meeting convenes at the spacious Las Vegas Hilton conference center, which will host both the technical and exhibit programs. The term "design automation" denotes a discipline which includes all users of computers for the design process in a variety of fields and for a variety of products. This year's program presents recent technical innovations in a broad spectrum of fields including design automation for both analog and digital circuits and VLSI systems.

From the conference chairman...

I would like to take this opportunity to invite you to the 23rd ACM/IEEE Design Automation Conference—the premiere conference in the fields of CAD/CAE/CAT and related disciplines.

The field of design automation continues to grow in size and technical scope. The ACM/IEEE Design Automation Conference strives to reflect this vitality; first, in its technical program, and second, in its presentation of selected vendor products to attendees.

Since the late 1970's, many of the important technical advances in design automation have begun in colleges and universities. In recognition of this trend, our Program Chairman this year is Don Thomas from Carnegie-Mellon University (now on sabbatical at IBM). The Program Chairman and the Program Committee have assembled an excellent technical program from over 300 submitted papers.

To permit more qualified vendors to exhibit their products at the conference, we have more than doubled the exhibit space over last year. This year, for the first time, we will be having sessions on Sunday to permit vendors to present their products in a more formal setting. Please give your comments on this and any other part of the conference to the Conference Committee—this is the best way that the conference can best serve the interests of you, the attendees.

Arrangements and transportation will be excellent; the size of the conference last year dictated the use of the Las Vegas Hilton—the largest hotel in the world. The Tuesday night dinner at Caesar's Palace promises again to be a night to remember.

The conference Committee welcomes everyone to Las Vegas and the 23rd ACM/IEEE Design Automation Conference

Dan Nash
Chairman

From the program chairman...

The primary goal of the DAC is to provide a high-quality technical program that meets the needs of the engineering community. To remain current, an engineer must be aware of both technical innovation and commercially available systems to aid in the design, test, and manufacture of circuits and VLSI systems. Thus, exhibit its remain an integral part of the DAC, but they are controlled to be in balance with and augment the technical program.

Because of the breadth of subject matter, the three-day program has been arranged so that technical papers in different disciplines are presented concurrently. Sessions are included in the subject areas of simulation, testing, hardware description languages, automatic and interactive placement and routing, silicon compilation, timing and design rule verification, human interaction, data path synthesis, expert systems, and special-purpose computing hardware for design tasks.

In addition, panel sessions and tutorials will address a broad spectrum of subjects. The tutorials include several presentations on parallel processing for design automation applications, built-in self-test, the application of expert systems to CAE, and automatic placement. The panels include discussions on yield modeling of VLSI circuits, implications for CAD of trends in device/process technology, and floor planning systems.

There are a number of sessions that look to be of special interest this year. Over the last several years, there has been considerable work in the area of developing language and design representation standards. In response to this, we will have tutorials on the VHDLIC Hardware Description Language (VHDL) and the Electronic Design Interchange Format (EDIF). Following these, there will be a panel discussing the progress toward their implementation and use. The tutorials and panel discussion will be held Tuesday morning.

In addition, two sessions will focus on design automation tools used in designing Hitachi's M-680H/682H high-end mainframe computers. These sessions will include papers overviewing the design automation system used, as well as papers on logic simulation, logic synthesis, delay analysis, and placement algorithms for optimizing delay for high-speed masterslice IC's.

Finally, there will be a session on logic synthesis in which the three papers will be followed by a short panel discussion. Included in the approaches to logic synthesis are both rule-based and programmed approaches. Some of the examples used in these papers were drawn from a common pool, allowing for better comparison of the different approaches.

Don Thomas
Program Chairman
Design Automation Conference Technical Program

All sessions will be held at the Las Vegas Hilton.

June 1986

Session Number: 01, Plenary
R 8:00-10:00am Rm A/B/C/D
Opening Remarks
J.D. Nash, Chairman; D. Yinger, Arrangements Chairman;
D. Thomas, Program Chairman

Awards
Comb Shaw, ACM Representative; D.Lambert, IEEE Representative

Keynote Address
R.M. Williams, IBM, Milford, CT

Session Number: 02, Approaches To Parallel Simulation
R 10:30-12:00pm Rm A
Chair/Organizer: R.A. Rutenbar, CMU
2.1 Fundamentals of Parallel Logic Simulation
R.J. Smith, II, MCC
2.2 Statistics on Logic Simulation *
K.F. Wong, M.A. Franklin, R.D. Chamberlain, B.L. Shing, Washington Univ.
2.3 Exploiting Parallelism in A Switch-Level Simulation Machine
E.H. Frank, Austek Microsystems, Australia

Session Number: 03, Database I
R 10:30-12:00pm Rm B
Chair/Organizer: N. Elias
3.1 A Version Server for Computer-Aided Design Data
R.H. Katz, UC Berkeley; M. Anwaruddin, Digital Equipment Corp.; E. Chang, UC Berkeley *
3.2 Semantics of CAD Objects for Generalized Databases
G.T. Nguyen, D. Rieu, Universite de Grenoble
3.3 DOS/II: A Storage System for Design Database
S. Weiss, K. Rozell, T. Rhys, A. Goldfain, MCC

Session Number: 04, Intelligent Systems
R 10:30-12:00pm Rm C
Chair: C. Tong, Rutgers Univ.
Organizer: A.C. Parker
4.1 A Design Utility Manager
A.C. Parker, D.W. Knupp, USCI
4.2 VLSI CAD Tool Integration Using the ULYSSES Environment
M.L. Bushnell, S.W. Director, CMU
4.3 An Expert System Paradigm for Design
F.D. Brewer, D.D. Gajski, Unio. of Illinois at Urbana

Session Number: 05, Tutorial: Perspectives on Parallel Processing for Design Automation A*:applications
T:1:30-2:30pm Rm A
Chair: Randel E. Bryant, CMU
5.1 Parallel Processing For Design Automation Applications
J.M. Hancock, S. Datta, Gupta, IBM Corp.

Session Number: 06, Logic Synthesis and Optimization
R 1:30-3:30pm Rm B
Chair/Organizer: A.J. DeGeus, GE Calma
6.1 SOCRATES: A System for Automatically Synthesizing and Optimizing Combinational Logic
D. Gregory, GE Calma; K. Bartlett, Univ. of Colorado; A. DeGeus, GE Calma; G. Hatchel, Univ. of Colorado
6.2 MACDAS: Multi-level AND-OR Circuit Synthesis Using Two-Variable Function Generators
T. Sasa, Osaka Univ.
6.3 Technology Adaptation in Logic Synthesis *
6.4 Panel: Future Directions in Logic Synthesis
R. Brayton, IBM Yorktown Heights, NY; J. Fox, GTE Labs, Waltham MA; D. Gregory, GE Calma, Research Triangle Park, NC; W. Joyner, IBM Yorktown Heights, NY; T. Sasa, Osaka Univ., Japan

Session Number: 07, Floor Planning and Compaction
R 1:30-3:30pm Rm C
Chair: A.E. Dunlop, AT&T Bell Labs
Organizers: Alfred E. Dunlop, Bryan Preas, Daniel Schweikert
7.1 A New Algorithm for Floorplan Design *
D.F. Wong, C.L. Liu, Unio. of Illinois at Urbana
7.2 A Linear Algorithm To Find A Rectangular Dual Of A Planar Triangulated Graph
S. Sahni, J. Bisker, Unio. of Minnesota
7.3 Two-Dimensional Compaction By "Zone Refining" *
H. Shin, A. Sangiovanni-Vincentelli, C.H. Sequin, UC Berkeley
7.4 MINPLEX—A Compactor That Minimizes The Bounding Rectangle and Individual Rectangles In A Layout
S.L. Lin, J. Allen, MIT

Session Number: 08, Towards Automated Interfaces
R 1:30-3:30pm Rm D
Chair: S.J. Mountford, MCC
Organizers: S.J. Mountford, F. Frome
8.1 GEMS—A Graphics Editor for MIMOLA Schematics
V.V. Venkateswaran, C.D. Wilcox, Honeywell Computer Sci., Ctr.
8.2 An Object-Oriented Visual Simulator for Microprogram Development
A. Sugimoto, S. Abe, M. Kuroda, Y. Kato, Mitsubishi Electric Corp.
8.3 A Monitor for Complex CAD Systems
A. DiManni, Centro Studi e Laboratori, Italy
8.4 Automating The Generation of Interactive Interfaces
K. Hammer, J. Hardin, T. Timmerman, D. Radin, MCC

Session Number: 09, Switch-Level Simulation
R 2:30-3:30pm Rm A
Chair/Organizer: R.E. Bryant, CMU
9.1 SIMMOS—A Logic/Timing Simulator For Digital CMOS VLSI
D. Adler, Motorola Semiconductor Israel
9.2 SLS—A Fast Switch Level Simulator For Verification and Fault Coverage Analysis

Session Number: 10, Electrical and Mixed-Mode Simulation
R 4:00-5:30pm Rm A
Chair: S.W. Director, CMU
Organizer: A.R. Newton
10.1 MOS Circuit Models In Network C *
W.S. Beckett, Univ. of Washington
10.2 CINNAMON: Coupled Integration and Nodal Analysis of MOS Networks
L. Vidigal, S.R. Nassif, S.W. Director, CMU
10.3 A Workstation-Based Mixed Mode Circuit Simulator
P. Oydyne, K. Nazareth, C. Christensen, Silicon Design Labs, Inc.

Session Number: 11, Logic Minimization and Verification
R 4:00-5:30pm Rm B
Chair: G.D. Hachtel, Unio. of Colorado
Organizer: A. DeGeus
11.1 Generating Essential Primes For A Boolean Function With Multiple-Valued Inputs
Y.S. Kuo, W.K. Chou, Inst. of Information Science Academia Sinica, Taiwan
11.2 A New Method For Verifying Sequential Circuits
K. Supowit, S.J. Friedman, Princeton Univ.
11.3 A Logic Verifier Based On Boolean Comparison
G. Odawara, M. Tomita, O. Okazawa, T. Ohia, Univ. of Tokyo

Session Number: 12, Timing Verification (I)
R 4:00-5:30pm Rm C
Chair/Organizer: R. Hitchcock, IBM Corp.
12.1 Reasoning About Digital Systems Using Temporal Logic
G. Venkatesh, Tata Inst. of Fundamental Research, Bombay, India; S. Bapat, Indian Inst. of Technology
12.2 SCAT—A New Timing Verifier In A Silicon Compiler System
M. Glesner, J.J. Schuck, R.B. Steck, Technical Univ. Darmstadt, F.R. Germany
12.3 An Accurate Delay Modeling Technique For Switch Level Timing Verification
S.H. Hwang, Y.H. Kim, A.R. Newton, UC Berkeley
Session Number: 13, Yield of VLSI Circuits: Myths vs. Reality
P 8:00-10:00 Rm C
Chair: A. Strojwas, CMU
Panel members:
D. Buss, T.J. C. Stapper, IBM, General Technology Div.; C. Beck, Sierra Semiconductor; T. Mangir, UCLA

Session Number: 14, Test Generation Techniques
R 8:00-10:00 Rm A
Chair: P.W. Horstmann, IBM Corp.
Organizers: S. DasGupta, P.W. Horstmann
14.1 Robust Test Generation Algorithm for Stuck-Open Fault in CMOS Circuits
M. Weieki, L. Xieting, Fudan Univ., Shanghai, China
14.2 Transistor Level Test Generation for Physical Failures in MOS Circuits
H.C. Shih, J.A. Abraham, Univ. of Illinois
14.3 An Effective Test Generation System for Sequential Circuits
R. Marlet, HHB Systems
14.4 A Heuristic Chip-Level Test Generation Algorithm

Session Number: 15, Control/Data Path Synthesis
R 8:00-10:00 Rm B
Chair/Organizer: A.C. Parker, USC
15.1 HAL: A Multi-Paradigm Approach To Automatic Data Path Synthesis
P.G. Paulin, J.P. Knight, Bell-Northern Research, Canada
15.2 A New Synthesis Algorithm For The MIMOLA Software System
P. Marwedel, Inst. fur Informatik und Praktische Mathematik der Universitat Kiel, F.R. Germany
15.3 Synthesis Of VLSI Systems With The CAMAD Design Aid
Z. Peng, Linkoping Univ., Sweden
15.4 Synthesis of Concurrent Modular Controllers From Algorithmic Descriptions
F. Ramming, Univ., Paderborn; R. Bruck, Univ., Dortmund; B. Klenjohann, T. Karhofer, Univ. Paderborn, F.R. Germany

Session Number: 16, VLSI Placement
R 8:00-10:00 Rm C
Chair: D.G. Schweikert, United Technologies Micro. Elect. Ctr.
Organizers: A. Dunlop, B. Preas, D. Schweikert
16.1 Simulated Annealing and Combinatorial Optimization
S. Sahni, S. Nahar, Univ. of Minnesota; E. Shragowitz, Control Data Corp.
16.2 Integrated Placing/Routing In Sliced Layouts
A. Szepieniec, Targent Systems Corp.
16.3 On The Relative Placement and The Transportation Problem For Standard-Cell Layout
F.M. Johannes, K.M. Just, J.M. Kleinans, Technische Uni. Munich
16.4 An Analysis Of Placement Procedures For VLSI Standard Cell Layout
Mark R. Hartoog, VLSI Technology Inc.

Session Number: 17, VHDL: The VHIC Hardware Description Language
T 8:00-9:00 Rm D
M. Shahdad, CAD Language Systems, Inc.

Session Number: 18, Tutorial: Electronic Design Interchange Format (EDIF)
T 9:00-10:00 Rm A
J.P. Eueich, Daisy Systems Corp.

Session Number: 19, Testing For Regular Structures
R 10:30-12:00 Rm R
Chair: S. Hirschhorn, GTE Labs
Organizers: S. DasGupta, P.W. Horstmann
19.1 A Unified Treatment of PLA Faults By Boolean Differences
W. Duerst, Inst. fur Theoretische Elektrotechnik-Universitat Hannover
19.2 A Design For Testability of PLA’s Using Statistical Cooling
M.L. Lichtig, E. Aarts, F. Beeneker, Phillips Research Labs, The Netherlands
19.3 Use Of The Subscripted DALG In Submodule Testing With Applications In Cellular Arrays
J.F. McDonald, M. Ladijai, W. Murray, Jr., D.-H. Ho, RIPI

Session Number: 20, CAD For Hitachi M-680H/682H
R 10:30-12:00pm Rm B
Chair: Y. Ohno, Hitachi, Ltd.—Kanagawa Works
20.1 Principles of Design Automation System For Very Large Scale Computer Design
Y. Ohno, M. Miyachi, N. Yamada, Hitachi, Ltd.—Kanagawa Works
20.2 An Extensive Logic Simulation Method Of Very Large Scale Computer Design
M. Miyoshi, Y. Ooshima, A. Sagiyama, N. Oonizuka, N. Amano, Hitachi, Ltd.—Kanagawa Works
20.3 Establishment of Higher Level Logic Design For Very Large Scale Computer

Session Number: 21, Panel: Implications for CAD of Trends in Device/Process Technology
P 10:30-12:00pm Rm C
Chair/Organizer: A.J. Goldfain, MCC

Session Number: 22, Panel: Computer Aided (CA) Tools Integration and Related Standards Development
P 10:30-12:00pm Rm D
Chair: R.J. Pachter, Sanders Associates, Inc.
Panelists:

Session Number: 23, Self-Test and Fault Tolerance
R 1:30-3:00pm Rm A
Chair: S. DasGupta, IBM Corp.
Organizers: S. DasGupta, P.W. Horstmann
23.1 Self-Testing With Correlated Faults
D.R. Tryon, IBM Japan Ltd.
23.2 Automatic Test Generation of Self-Test Programs—A New Feature Of The MIMOLA Design System
G. Krager, Siemens AG, F.R. Germany
23.3 An Algorithm For Efficient Spare Allocation In Reconfigurable Arrays
W.K. Fuchs, S.-Y. Kao, Univ. of Illinois

Session Number: 24, CAD for Hitachi M-680H/682H, Continued
R 1:30-3:00pm Rm B
Chair: Y. Ohno, Hitachi, Ltd.—Kanagawa Works
24.1 Incremental Logic Synthesis Through Gate Logic Structure Identification
K. Ishihara, T. Shinsha, T. Kuro, Y. Sakataya, Hitachi Ltd.—Kanagawa Works; J. Koshibuda, Hitachi Software Eng., Ltd., Yokohama, Japan
24.2 A Delay Analysis System To Remove All Delay Failures In Large Scale Computer Design
24.3 Efficient Placement Algorithms Optimizing Delay For High Speed ECL Masterslice LSIs

Session Number: 25, Layout Verification
R 1:30-3:00pm Rm C
Chair: E.T. Grinthal, AT&T Bell Labs
Organizer: P. Agrawal
25.1 A Time and Space Efficient Net Extractor
S. Sahni, S. Nahar, Univ. of Minnesota
25.2 Extraction of SPICE Circuit Models From Symbolic Gate-Matrix Layout with Pruning
C.G. Lin-Hendel, R.D. Freeman, AT&T Bell Labs; S. M. Kang, M.L. Newby, Univ. of Illinois at Urbana
25.3 A Technology Independent Approach To Hierarchical IC Layout Extraction
A. Bootehsaz, R.A. Coitrell, UMIST, Manchester, England

Session Number: 26, Silicon Layout
R 1:30-3:00pm Rm D
Chair: E. Yoffe, IBM T.J. Watson Research Ctr.
Organizer: A. Dunlop, B. Preas, D. Schweikert
26.1 TIMBERWOLF3.2: A New Standard Cell Placement and Global Routing Package
C. Sechen, A. Sangiovanni-Vincentelli, UC Berkeley
26.2 VANGUARD: A Chip Physical Design System
P.S. Hauge, E.J. Yoffe, IBM T.J. Watson Research Ctr.
26.3 Automated Layout Synthesis In The YASC Silicon Compiler
D.E. Krekelberg, G.E. Sobelman, E. Shragowitz, Control Data Corp.; L.-S. Lin, Univ. of Minnesota
Session Number: 40, Printed Circuit Board (PCB) Routing (1)
R 10:30-12:00pm Rm D
Chair: P.S. Hosinger, IBM Corp.
Organizer: R.B. Hitchcock
40.1 A New Approach To Multi-Layer PCB Routing
H.C. Du, J.F. Naveda, K.C. Chang, Univ. of Minnesota
40.2 A Preprocessor For Layer Assignment Problem
H.C. Du, K.C. Chang, Univ. of Minnesota
40.3 Near Optimal n-Layer Channel Routing
H.C. Du, R.J. Enbody, Univ. of Minnesota

Session Number: 41, Silicon Compilation
R 1:30-3:30pm Rm A
Chair: J. Fox, GTE Labs
Organizer: D. Gajski
41.1 Principles Of The Syco Compiler
A. Jeraraya, R. Jamier, B. Courtois, TIM3-Img/INPG, France
41.2 DATAPATH; A CMOS Datapath Silicon Assembler
T. Marshburn, R. Brown, J. Lui, D. Cheung, G. Lum,
P. Cheng, Hewlett-Packard
41.3 An Intelligent Module Generator Environment
P. Six, L. Claesen, J. Rabaey, H. De Man,
IMEC—VSDM Division, Belgium
41.4 HAPPY; A Chip Compiler Based On Double Level Metal Technology

Session Number: 42, Database II
R 1:30-3:30pm Rm B
Chair: R. Katz, UC Berkeley
Organizer: N. Elias
42.1 An Object Oriented, Procedural Database For VLSI Chip Planning
W. Wolf, AT&T Bell Labs
42.2 An Automated Database Design Tool Using The ELKA Conceptual Model
M.C.J. Sustarta, Inst. de Investigaciones Elec., Mexico;
A. P. Buchmann, National Univ. of Mexico
42.3 A Database Interface For An Integrated CAD System
C. Jullien, A. LeBlond, Centre National d’Etudes des Telecommunications, France
42.4 Rules-Based Object Clustering: A Data Structure For Symbolic VLSI Synthesis And Analysis
R.P. Larsen, Rockwell International Corp.

Session Number: 44, Printed Circuit Board (PCB) Routing (2)
R 1:30-3:30pm Rm D
Chair: P.S. Hosinger, IBM Corp.
44.1 Router System For Printed Wiring Boards Of Very High Speed, Very Large-Scale Computers
T. Tada, A. Hamafusa, Fujitsu Ltd.
44.2 Global Forced Hierarchical Router
J. Kesenenich, G. Jackoway, Hewlett-Packard
44.3 Hierarchical Dynamic Power
K. Kawamura, H. Shiraishi, M. Umeda, Fujitsu Laboratories Ltd.
44.4 A Parameter Driven Router
J.W. Smith, V.S. Bobba, Univ. of Georgia

Session Number: 43, Timing Verification (3)
R 1:30-3:30pm Rm C
Chair: J.L. Rivero, IBM Corp.
43.1 Simulating and Controlling the Effects of Transmission Line Impedance Mismatches
R.E. Carrigh, Martin Marietta Orlando Aerospace
43.2 A Delay Test System For High Speed Logic LSIs
K. Kishida, F. Shirotori, Y. Iemoto, S. Isiyama, T. Hayashi, Hitachi Ltd.
43.3 Panel: Future Directions in Timing Verification

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New Product/Applications Program
Sunday, June 29, 1986
Las Vegas Hilton

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<td>2:00 p.m.</td>
<td>Microsim</td>
<td>Electr. Eng. Software</td>
<td>Tektronix</td>
<td>Shiva</td>
<td>SDA</td>
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<td>2:30 p.m.</td>
<td>Silvar Lisco</td>
<td>Silicon Solutions</td>
<td>Seattle Silicon</td>
<td>Quantic Labs</td>
<td>Analog Des. Tools</td>
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<td>3:00 p.m.</td>
<td>DEC</td>
<td>Praxis Systems</td>
<td>Telesis Systems</td>
<td>Viewlogic</td>
<td>VIA Systems</td>
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<td>3:30 p.m.</td>
<td>Hewlett-Packard</td>
<td>Cadre Tech.</td>
<td>FutureNet</td>
<td>Xerox</td>
<td>IBM</td>
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<td>4:00 p.m.</td>
<td>Valid Logic</td>
<td>Teradyne</td>
<td>Data I/O</td>
<td>Octal</td>
<td>Phoenix Data Syst.</td>
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<td>4:30 p.m.</td>
<td>ENDOT</td>
<td>ECAD</td>
<td>VLSI Technology</td>
<td>MIPS</td>
<td>HiLevel Tech.</td>
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<td>5:00 p.m.</td>
<td>Floating Pt. Syst.</td>
<td>Meta-Software</td>
<td>Integrated Meas. Syst.</td>
<td>Control Data</td>
<td>Racal-Redac</td>
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<td>Lattice Logic</td>
<td>Aida</td>
<td>Computevision</td>
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<td>6:00 p.m.</td>
<td>Zycad</td>
<td>Scientific Calc.</td>
<td>Silicon Des. Labs</td>
<td>CADAM</td>
<td>Convex</td>
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<td>6:30 p.m.</td>
<td>Logic Automation</td>
<td>Clarity Syst.</td>
<td>Daisy Syst.</td>
<td>Genrad</td>
<td>Applied Microtech</td>
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<td>7:00 p.m.</td>
<td>HHB Syst.</td>
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List of Exhibitors

All exhibits will be held at the Las Vegas Hilton.

Exhibit hours:

- **Sunday, June 29**: 2:00 p.m. to 7:00 p.m.
- **Monday, June 30**: 10:30 a.m. to 5:00 p.m.
- **Tuesday, July 1**: 10:30 a.m. to 5:00 p.m.
- **Wednesday, July 2**: 9:00 a.m. to 3:00 p.m.

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