First International Workshop on VLSI Design

H.N. Mahabala, IIT, Madras
V.D. Agrawal, AT&T Bell Labs

The First International Workshop on VLSI Design, held in Madras, India, December 26-28, 1985, was a surprising success. Most of the 98 attendees showed strong interest in coming back to another such event if scheduled a year later. The workshop was sponsored by the Computer Society of India (CSI) and the IEEE India Council.

In opening the workshop, CSI President O.P. Mehra cited VLSI design as a more challenging activity for engineers than other maintenance-type jobs. He applauded the Indian government's move to relax computer import restrictions, saying that the current plan for increasing productivity through computerization would work if more computers and trained personnel were available. Mehra put the 1985 production of computers in India at 10,000 and urged the government to fund several VLSI design centers to accelerate growth.

The workshop program, which was preceded by a one-day tutorial on VLSI design, was divided into nine sessions. The first session included three papers on the state of the art in VLSI design, testing, and technology, respectively. Other sessions were devoted to papers on VLSI architectures, programmable logic arrays, silicon compilers, simulation, test generation, design for testability, routers, and physical design.

In one of three papers in the session on silicon compilers, V.P. Srinivasan and A.M. Despain of the University of California, Berkeley, described their continuing work on a VLSI chip generator using dataflow methodology. The physical design session included two papers from the Indian Telephone Industries describing their symbolic layout system. In the same session, an interconnect verification program now in use at Digital Equipment Corporation was described by K.L. Kodandapani.

A paper by J. Patel of the University of Illinois, in which he described several heuristics for speeding up the PODEM algorithm, generated very active discussion in the session on test generation. In the same session, authors from Siemens in Germany presented a functional testing approach and a partitioning architecture to make testing practical. In the session on simulation, discussion centered around three papers on AT&T Bell Labs' mixed-mode simulator; another mixed-mode simulator, MOSIMER, developed by the Indian Institute of Technology at Kanpur and implementing their new latency exploitation algorithm; and recent advances in hardware accelerators described by P. Agrawal.

Perhaps the most interesting workshop session was "VLSI in India." A number of organizations were invited to summarize their expertise and tools. In terms of tool development, the Tata Institute of Fundamental Research in Bombay was the clear winner. Researchers there described their work on switch-level simulators, circuit extraction, design rule checkers, synthesis using temporal logic, fault simulators, and layout. Another presentation from the Semiconductor Complex in Chandigarh reported in their complete design center/silicon foundry operation. Starting with customers' schematics, they have designed at least half a dozen chips that are now in production.

Perhaps the most complete design and development facility in India exists at the Indian Telephone Industries in Bangalore. They are developing a VLSI CAD package based on their printed circuit board design package—named NIRMAN—that is now marketed in India. This CAD group is also involved in technology development using their recently-completed pilot MOS processing line. Several VLSI user groups present at the workshop voiced their concern about the available semicomplex process being too expensive with long turnaround. They asked for greater user participation in design center activities.

In all, 25 formal papers were presented at the workshop. A copy of the Proceedings is available from: Prof. H.N. Mahabala, Dept. of Computer Sciences and Engineering, Indian Institute of Technology, Madras 600036, India.

Third ICCAD an unqualified success

The Third International Conference on Computer-Aided Design (ICCAD 85), held in Santa Clara, California, Nov. 18-21, 1985, was an unqualified success despite the economic slump affecting many semiconductor and systems manufacturers. The conference's popularity attests to the timeliness and quality of the technical program: For the second straight year, combined conference/tutorials attendance exceeded 1000. Both the technical sessions and the evening panel sessions were well attended, and high interest in the tutorials meant some prospective attendees had to be turned away.

Below are some of the highlights of the conference, grouped according to technical area.

Test. The papers on test topics provided a diverse qualitative mix of works, from theoretical (such as "C-testability of Two-dimensional Arrays," by Hasan Elhuni et al. of the University of Minnesota) to applied ("An Integrated Design for Testability System," by Francis C. Wang et al. of Tektronix).

One of the most difficult problems in test is automatic test pattern generation, and two papers at the conference dealt with this subject. Ki Soo Hwang and Ray Mercer of the University of Texas tackled the problem by treating internal fanout points as pseudo inputs and ordering the dependency of these points upon one another and other primary inputs. Thus, the circuit is transformed into a pseudo-tree structure. The rest of the algorithm consists of intersection operations on the cubical representation of fanout constraints. The second paper, by Scott Robinson and John Shen of CMU, presented a switch-level ATPG algorithm aimed at CMOS combinational circuits. This approach involves representing logic components in switch-level models, and then precomputing the information necessary for a D-algorithm-like ATPG approach.

Two papers addressed another difficult, and perhaps more pressing, problem: fault simulation. Takao Nishida et al. of Hitachi presented several shortcuts that have resulted in an order-of-magnitude decrease in runtime over a traditional concurrent fault simulator. Some of these shortcuts, such as not propagating a fault if it cannot possibly be detected, are obvious and probably implemented in most existing fault simulators. Hsi-Ching Shih, Joseph Rahme, and Jacob Abraham of the University of Illinois described a fault simulator that includes timing information. That is, MOS-type failures can be injected and the result on output timing simulated.

Layout. The symbolic layout approach and associated compaction techniques were the focus of a number of design systems and subsystems. M.C. Revett of British Telecom Research Labs described a working CAD system that integrates symbolic layout and compaction tools with functional design (simulation) tools. The floor-planning process lets the designer input structural interconnections, estimated block sizes, and topological relationships to allow the functional and physical design phases to proceed in parallel. The cell
design process is based on the virtual grid symbolic layout approach, which aids correct layout while maintaining technology flexibility.

Authors from IBM and NEC discussed other systems employing symbolic layout approaches. Atsushi Kurosawa et al. from NEC detailed how compaction techniques are used to generate final layouts of a density comparable to manual designs. NEC's system reportedly reduces overall design time by a factor of two.

Stephen Poslusznny from IBM described practical features that aid compaction in a hierarchical layout compaction system. In a related paper, David Deutsch from AT&T Bell Communications research described another useful application of compaction—compaction following channel routing—and discussed a possible extension to gridless routing.

Two papers focused on interesting work in "greedy" routers. Peter Brueell and Paul Sun from the Microelectronics and Computer Technology Corporation described an 11-track solution in three layers to Deutsch's difficult channel example. J.R. Stenstrom and R.M. Mattheyes from GE showed the potential degradation in area efficiency when a switch-box router is applied to a channel-routing problem.

An improved approach to mapping the Lee algorithm onto a parallel-processing architecture was presented by Tatsu6 Ohtsuki et al. of Waseda University. The key to their algorithm lies in mapping only the wavefront to the parallel processors, resulting in O(N) processor and time requirements for finding a path on an \( N \times N \) grid plane.

In the area of module composition tools, Steve Law and John Mosby from SDA Systems described a module compiler compiler, which employs graphical and procedural means allowing designers to define their own module compilers for building most macro-structures used in VLSI processors.

Simulation. ICCAD 85 included papers in all areas of simulation, including process/device, circuit-level, gate, and functional-level categories.

Waveform relaxation, or WR, techniques for bipolar circuits have been relatively unsuccessful because the coupling between the nodes of the circuits varies by orders of magnitude. Guy Marong and Alberto Sangiovanni-Vincentelli from the University of California at Berkeley described a dynamic partitioning scheme that makes the WR method significantly faster (while maintaining accuracy) than standard circuit simulation techniques.

Sani Nassif and Steve Director from CMU presented a new approach for simulating cell-based MOS designs. Macromodes of regular individual cells are generated analytically, and an event-driven, waveform-based simulator uses the macromodelled cells. The authors claimed to achieve circuit-level accuracy with logic-level speed.

Ping Yang from Texas Instruments presented a scheme for efficiently ordering the matrix equations obtained in the modified nodal formulation approach. A partitioning technique allows complete flexibility in reordering the matrix equations while guaranteeing that no zero-value pivots are generated. This near-optimum reordering scheme reduces the matrix operations for large circuit simulations by a factor of 3 to 400.

Device-level statistical models for MOSFETs were also popular. S. Liu from Bell Laboratories and K. Singhal from the University of Waterloo described a compact model that simulates the statistical variations in device characteristics for seven critical process parameters. A noise model is used to represent process variations and a combination of 1-D physical analysis, multi-parameter linear regression, and single-parameter non-linear regression is used to relate these variations to device model parameters.

Simulation for yield optimization was another popular subject. H. Walker and Director from CMU explained how they apply Monte Carlo techniques to place random catastrophic point defects on a chip layout and determine what circuit faults have occurred. This information is then used to predict yield, optimize design rules, evaluate redundancy, and generate test vectors.

Timing analysis attracted a great deal of interest. Bernard Murphy, et al. of SDA presented a mixed-level timing analyzer that allows estimation of timing at the transistor level or at the block level. Input for the program can be taken from schematics or layouts. Critical path information is back-annotated to the design for viewing or to guide other tools in the CAD system.

Systems. The systems area covered topics including databases and artificial intelligence, compilers, module generators, synthesis systems, hardware accelerators, and simulated annealing.

Databases and artificial intelligence. Among the interesting presentations in the databases and artificial intelligence area was the paper by George Clark and Rich Zippel discussing the SCHEMA system developed at MIT. The SCHEMA system provides an integrated environment for all aspects of the synthesis and analysis of electronics designs from PC boards through circuit and mass design of VLSI devices. The SCHEMA system in its present form illustrates the powerful user interface and database environment that can be constructed using state-of-the-art AI techniques.

The use of expert systems is becoming more and more common in designing integrated circuits. Robert Bowman and David Lane proposed using a knowledge-based design system called PROASIC for designing analog ICs. Designing analog circuits is much more complicated than designing digital circuits, and the initial efforts by the authors in applying expert system concepts to the design of CMOS operational amplifiers indicates the potential of expert systems in the analog area.

Hardware accelerators. The trend to design special purpose hardware accelerators for specific VLSI design tasks is well known and was illustrated by several papers at ICCAD 85. In examining the use of accelerators with workstations, Gary Catlin and Bill Paseman discussed the architecture of the dataflow accelerator used in the Daisy Megalogician. While not achieving the speed available on much more expensive hardware accelerators, this particular board can achieve a 100-percent speedup and handle 1 million gates in a workstation environment.

Simulated annealing. Simulated annealing, introduced by researchers at IBM Yorktown for solving combinatorial optimization problems, has received much attention over the past several years. New applications and modifications to simulated annealing were also presented at the conference. H. Fleisher et al. presented a technique for using simulated annealing as a logic optimization tool. This technique combines the decomposition, minimization, implication sharing and bit partitioning techniques used in other logic optimization systems, and provides a method for transforming Boolean functions by annealing. This technique promises to allow the global minimum of the implementation of a Boolean function to be achieved using the techniques of simulated annealing.

Compilation, generation, and synthesis. By far the greatest number of papers in the systems area were those associated with various synthesis, generation, and silicon compilation techniques.

Cell synthesis systems often form the basis of complete system compilation systems. Meng-Lin Yu and William Kubitz, in separate presentations, discussed the Asel cell synthesis system from the University of Illinois. The key feature of this system is its ability to specify structural constraints on the cells being synthesized. George Mei and Wentai Liu considered the synthesis of data paths with a system that allows constraints on the number of operators which can be used to realize the data path. In the unconstrained case, their techniques have produced better results than those previously available in the area.

Typical silicon compilation techniques are concerned with the construction of synchronous digital systems. Masaharu Hirayama from Mitsubishi presented a silicon compilation system based upon asynchronous architectures.

Application-specific ICs are becoming increasingly important. At the same time, compilation of these integrated circuits is receiving much attention. An important application area is in signal processing, and two papers were presented on the subject. Jeffrey Jasica et al. of General Electric's Corporate R&D Center presented a bit-serial compilation system for designing highly pipelined signal processing systems. Robert Owens and Mary Jane Irwin from Penn State University presented a high-
level interactive system for designing at the layout level of various signal processing operations. Their scheme was based on special-purpose, digit-on-line digit serial elements.

In cell and module synthesis, it often becomes important to resize transistors in order to achieve timing, area or power performance constraints. J.P. Fishburn and A.E. Dunlop of AT&T Bell Laboratories presented a program called Tilos, using techniques of polynomial programming to formulate and solve the transistor resizing problem. Although this is one of several techniques that have been presented in the past few months, the authors’ approach is by far the most mathematically elegant of those available to date. In addition to its elegance, the performance seems to be excellent as well.

**Panel sessions.** This year, two evening panel sessions were held in parallel; both sessions were well-attended with approximately 350 attendees each.

In “Is There Life in SPICE?” the panel unanimously concluded that SPICE could very well be around for another 10 years. The term “alphabet SPICE” was used for variations of SPICE sold and supported by vendors, and the panel acknowledged the service performed by these vendors for companies not wishing to support SPICE internally.

Participants in the second panel, “Intelligent CAD Software: Current Status, Future Prospects,” concluded that there are no currently truly “intelligent” CAD programs, nor will there likely be any in the near future. (A true AI program must be able to learn.) The panel further concluded that future successful AI-based CAD systems will require a mixture of knowledge-based and algorithmic techniques.

**Tutorials/workshop.** Four all-day tutorials and one all-day workshop were held the day prior to the start of ICCAD 85’s technical sessions. The tutorials were limited to 75 attendees each to encourage discussion; each filled up early, and some late registrants were unable to attend.

Javad Khakhz, Min-Yu Hsueh, Brian Biehl, Mur Daniel, Hal Daseking, Mike Lightner, and Jerry Werner contributed to this report.

**ACM/IEEE 23rd Design Automation Conference set for June**

The 23rd ACM/IEEE Design Automation Conference will be held June 29-7uly 2, 1986, in Las Vegas, Nevada. An estimated 4000 attendees are expected when the meeting convenes at the spacious Las Vegas Hilton conference center, which will host both the technical and exhibit programs.

The term “design automation” denotes a discipline which includes all uses of computers for the design process in a variety of fields and for a variety of products. This year’s program presents recent technical innovations in a broad spectrum of fields including computer-aided design, computer-aided test, computer-aided manufacture, and computer-aided engineering. A wide range of application fields is covered, including design automation for both analog and digital circuits and VLSI systems.

The primary goal of the DAC is to provide a high-quality technical program that meets the needs of the engineering community. To remain current, an engineer must be aware of both technical innovation and commercially available systems to aid in the design, test, and manufacture of circuits and VLSI systems. Thus, exhibits remain an integral part of the DAC, but they are controlled to be in balance with and augment the technical program.

**DAC Program**

**Session Number: 03, Database I**
R 10:30-12:00pm Rm B
Chair/Organizer: N. Elias
3.2 Semantics of CAD Objects for Generalized Databases G.T. Nguyen, D. Rieu, Universite de Grenoble
3.3 DOSS; A Storage System for Design Database S. Weiss, K. Rotzeli, T. Rhyne, A. Goldkamp, MCC

**Session Number: 04, Intelligent Systems**
R 10:30-12:00pm Rm C
Chair: C. Tong, Rutgers Univ. Organizer: A.C. Parker
4.1 A Design Utility Manager A.C. Parker, D.W. Knapp, USC
4.2 VLSI CAD Tool Integration Using The ULYSSES Environment M.L. Bushnell, S.W. Director, CMU
4.3 An Expert System Paradigm for Design F.D. Brewer, D.D. Gajski, Univ. of Illinois at Urbana

**Session Number: 05, Tutorial: Perspectives on Parallel Processing for Design Automation Applications**
T 1:30-2:30pm Rm A
Chair: Randal E. Bryant, CMU
5.1 Parallel Processing For Design Automation Applications J.M. Hancock, S. DasGupta, IBM Corp.

**Session Number: 06, Logic Synthesis and Optimization**
R 1:30-3:30pm Rm B
Chair/Organizer: A.J. DeGeus, GE Calma
6.1 SOCRATES; A System for Automatically Synthesizing and Optimizing Combining Logic
D. Gregory, GE Calma; K. Bartlett, Univ. of Colorado; A. De Geus, GE Calma; G. Hatchel, Univ. of Colorado
6.2 MACDAS; Multi-level AND-OR Circuit Synthesis Using Two-Variable Function Generators T. Sasaki, Osaka Univ.
6.4 Panel: Future Directions in Logic Synthesis R. Brayton, IBM Yorktown Heights, NY; J. Fox, GTE Labs, Waltham MA; D. Gregory, GE Calma, Research Triangle Park, NC; W. Joyner, Jr., IBM Yorktown Heights, NY; T. Sasaki, Osaka Univ., Japan

**Session Number: 07, Floor Planning and Compaction**
R 1:30-3:30pm Rm C
Chair: A.E. Dunlop, AT&T Bell Labs Organizers: Alfred E. Dunlop, Bryan Preas, Daniel Schweikert
7.1 A New Algorithm For Floorplan Design * D.F. Wong, C.L. Liu, Univ. of Illinois at Urbana
7.2 A Linear Algorithm To Find A Rectangular Dual Of A Planar Triangulated Graph S. Sabini, J. Bhaker, Univ. of Minnesota
7.3 Two-Dimensional Compaction By “Zone Refining” H. Shin, A. Sangiovanni-Vincentelli, C.H. Sequin, UC Berkeley
7.4 MINPLEX—A Compiler That Minimizes The Bounding Rectangle and Individual Rectangles In A Layout S.L. Lin, J. Allen, MIT

**Session Number: 08, Towards Automated Interfaces**
R 1:30-3:30pm Rm D
Chair: S.J. Mountford, MCC Organizers: S.J. Mountford, F. Fronce
8.3 A Monitor for Complex CAD Systems A. Di Janni, Centro Studi e Laboratori, Italy
8.4 Automating The Generation of Interactive Interfaces K. Hammer, J. Hardin, T. Timmerman, D. Radin, MCC

**Session Number: 09, Switch-Level Simulation**
R 2:30-3:30pm Rm A
Chair/Organizer: R.E. Bryant, CMU
9.1 SIMMOS--A Logic/Timing Simulator For Digital CMOS VLSI D. Adler, Motorola Semiconductor Israel

* Asterisk denotes "Best Paper" nominee

April 1986
Session Number: 10, Electrical and Mixed-Mode Simulation
R 4:00-5:30pm Rm A
Chair: S.W. Director, CMU
Organizer: A.R. Newton
10.1 MOS Circuit Models In Network C
W.S. Beckett, Univ. of Washington
10.2 CINNAMON: Coupled Integration and Nodal Analysis of MOS Networks
L. Vidigal, S.R. Nassif, S.W. Director, CMU
10.3 A Workstation-Based Mixed Mode Circuit Simulator
P. Odyrnya, K. Nazareth, C. Christensen, Silicon Design Labs, Inc
Session Number: 11, Logic Minimization and Verification
R 4:00-5:30pm Rm B
Chair: G.D. Hachtel, Univ. of Colorado
Organizer: A.DeGeus
11.1 Generating Essential Primes For A Boolean Function With Multiple-Valued Inputs
Y.S. Kuo, W.K. Chou, Inst. of Information Science Academia Sinica, Taiwan
11.2 A New Method For Verifying Sequential Circuits K. Supowit, S.J. Friedman, Princeton Univ.
11.3 A Logic Verifier Based On Boolean Comparison G. Odawara, M. Tomita, O. Okaizawa, T. Ohta, Univ. of Tokyo
Session Number: 12, Timing Verification (I)
R 4:00-5:30pm Rm C
Chair/Organizer: R. Hitchcock, IBM Corp.
12.1 Reasoning About Digital Systems Using Temporal Logic G. Venkatesh, Tata Inst. of Fundamental Research, Bombay, India; S. Bapat, Indian Inst. of Technology
12.2 SCAT—A New Timing Verifier In A Silicon Compiler System M. Glesner, J.J. Schuck, R.B. Steck, Technical Univ. Darmstadt, F.R. Germany
12.3 An Accurate Delay Modeling Technique For Switch Level Timing Verification S.H. Huang, Y.H. Kim, A.R. Newton, UC Berkeley
Session Number: 13, Yield of VLSI Circuits: Myths vs. Reality
P 4:00-5:30pm Rm D
Chair: A.J. Strowzas, CMU
Panel members:
D. Buss, T.C. Snapper, IBM, General Technology Div.; C. Beck, Sierra Semiconductor; T. Mangir, UCLA
Session Number: 14, Test Generation Techniques
R 8:00-10:00am Rm A
Chair: P.W. Horstmann, IBM Corp.
Organizers: S. DaGupta, P.W. Horstmann
14.1 Robust Test Generation Algorithm For Steck Op-Amp in CMOS Circuits M. Weiwei, L. Xieting, Fudan Univ., Shanghai, China
14.2 Transistor Level Test Generation For Physical Failures in MOS Circuits H.C. Shih, J.A. Abraham, Univ. of Illinois
14.3 An Effective Test Generation System For Sequential Circuits R. Markey, HBO Systems
Session Number: 15, Control/Data Path Synthesis
R 8:00-10:00am Rm B
Chair/Organizer: A.C. Parker, USC
15.1 HAL: A Multi-Paradigm Approach To Automatic Data Path Synthesis P.G. Pauls, J.P. Knight, Bell-Northern Research, Canada
15.2 A New Synthesis Algorithm For The MIMOLA Software System P. Marenfeld, Inst. fur Informatik und Praktische Mathematik der Universitat Kiel, F.R. Germany
15.3 Synthesis Of VLSI Systems With The CAMAD Design Aid Z. Peng, Linkoping Univ., Sweden
15.4 Synthesis of Concurrent Modular Controllers From Algorithmic Description F. Ramming, Univ. Paderborn; R. Brack, Univ. Dortmund; B. Kleijnhoven, T. Katohe, Univ. Paderborn, F.R. Germany
Session Number: 16, VLSI Placement
R 8:00-10:00 Rm C
Chair: D.G. Schweikert, United Technologies Micro. Elect. Ctr.
Organizers: A. Dunlop, B. Preas, D. Schweikert
16.1 Simulated Annealing and Combinational Optimization S. Saha, N. Sahr, Univ. of Minnesota; E. Shragowitz, Control Data Corp.
16.2 Integrated Placing/Routing In Sliced Layers A. Seepieniec, Tanger Systems Corp.
16.3 On The Relative Placement and The Transportation Problem For Standard-Cell Layout F.M. Johannes, K.M. Just, J.M. Kleinhaus, Technische Univ. München
16.4 An Analysis Of Placement Procedures For VLSI Standard Cell Layout Mark R. Hartoog, VLSI Technology Inc.
Session Number: 17, VHDL: The VHSC Hardware Description Language T 8:00-9:00 Rm D
M. Shahdad, CAD Language Systems, Inc.
Session Number: 18, Tutorial: Electronic Design Interchange Format (EDIF)
T 9:00-10:00 Rm D
J.P. Eichir, Daisy Systems Corp.
Session Number: 19, Testing For Regular Structures
R 10:30-12:00pm Rm A
Chair: S. Hirschhorn, GTE Labs Organizers: S. DaGupta, P.W. Horstmann
19.1 A Unified Treatment Of PLA Faults By Boolean Differences W. Daen, Inst. fur Theoretische Elektrotechnik- Univ. Hannover
19.2 A Design For Testability Of PLAs Using Statistical Cooling M.L. Lighart, E. Aarts, F. Beender, Philips Research Labs, The Netherlands
19.3 Use Of The Subscribed DALG In Submodule Testing With Applications In Cellular Arrays J.F. McDonald, M. Lajdaj, W. Murray, Jr., D.H. Ho, RPI
Session Number: 20, CAD For Hitachi M-680H/682H
R 10:30-12:00pm Rm B
Chair: Y. Ohno, Hitachi, Ltd.—Kanagawa Works
20.1 Principles of Design Automation System For Very Large Scale Computer Design Y. Ohno, M. Miyoshi, N. Yamada, Hitachi, Ltd.—Kanagawa Works
20.2 An Extensive Logic Simulation Method Of Very Large Scale Computer Design M. Miyoshi, Y. Ooshima, A. Sugiyama, N. Onitsuka, N. Amano, Hitachi, Ltd.—Kanagawa Works
20.3 Establishment Of Higher Level Design For Very Large Scale Computer Y. Tsuchiya, M. Morita, Y. Ikiyama, Hitachi, Ltd.—Kanagawa Works; S. Umatani, T. Tanagita, T. Mori, T. Tourmi, Hitachi Computer Engineering, Ltd.
Session Number: 21, Panel: Implications for CAD of Trends in Device/Process Technology
P 10:30-12:00pm Rm C
Chair/Organizer: A.J. Goldfinen, MCC
Session Number: 22, Panel: Computer Aided (CA) Tools Integration and Related Standards Development
P 10:30-12:00pm Rm D
Chair: R.J. Pachter, Sanders Associates, Inc.
Session Number: 23, Self-Test and Fault Tolerance
R 1:30-3:00pm Rm A
Chair: S. DaGupta, IBM Corp.
Organizers: S. DaGupta, P.W. Horstmann
23.1 Self-Testing With Correlated Faults D.R. Tryon, IBM Japan Ltd.
23.2 Automatic Test Generation Of Self-Test Programs—a New Feature Of The MIMOLA Design System G. Kruger, Siemens AG, F.R. Germany
23.3 An Algorithm For Efficient Sparse Allocation In Reconfigurable Arrays W.K. Fuchs, S.-Y. Kuo, Univ. of Illinois
Session Number: 24, CAD for Hitachi M-680H/682H, continued
R 1:30-3:00pm Rm B
Chair: Y. Ohno, Hitachi, Ltd.—Kanagawa Works
24.2 A Delay Analysis System To Remove All Delay Failures In Large Scale Computer Design K. Takizawa, Hitachi, Ltd.—Kanagawa Works; R. Toyoshima, Y. Takiguchi, K. Matsumoto, H. Hongou, Hitachi Computer Eng., Ltd.; M. Hashimoto, R. Kamikawa, Hitachi Ltd.—Tokyo
Session Number: 25, Layout Verification
R 1:30-3:00pm Rm C
Chair: E.T. Grinthal, AT&T Bell Labs
Organizer: P. Agrawal
25.1 A Time and Space Efficient Net Extractor S. Sahni, N. Nahar, Univ. of California
25.2 Extraction of SPICE Circuit Models From Symbolic Gate-Matrix Layout With Pruning C.G. Lin-Hendel, R.D. Freeman, AT&T Bell Labs; S. Kang, M.L. Newby, Univ. of Illinois at Urbana
25.3 A Technology Independent Approach To Hierarchical IC Layout Extraction A. Boothbeatt, R.A. Cottrell, UMIST, Manchester, England
Session Number: 26, Silicon Layout
R 1:30-3:00pm Rm D
Chair: E. Yoffa, IBM T.J. Watson Research Ctr.
Organizer: A. Dunlop, B. Preas, D. Schweikert
26.1 TIMBERWOLFE3.2: A New Standard Cell Placement and Global Routing Package C. Seelen, A. Sangiovanni-Vincentelli, UC Berkeley
26.3 Automated Layout Synthesis In The YASC Silicon Compiler D.E. Krekelberg, G.E. Sobelman, E. Shragowitz, Control Data Corp.; L.-S. Lin, Univ. of Minnesota
Session Number: 27, Data Path Synthesis
R 3:30-5:30pm Rm A
Chair: L. Hafer, Simon Fraser Univ.
Organizer: A.C. Parker, USC
27.1 Sehwa: A Program for Synthesis of Pipelines N. Park, A.C. Parker, USC
27.2 MAHA: A Program for Datapath Synthesis A.C. Parker, J. Pizarro, M. Milner, USC
27.3 PLEST: A Program For Area Estimation Of VLSI Integrated Circuits A.C. Parker, F.J. Kurdi, USC
27.4 Using Bottom Up Design Techniques In The Synthesis Of Digital Hardware From Abstract Behavioral Description M.C. McFarland, S.J., AT&T Bell Labs
Session Number: 28, VLSI Routing
R 3:30-5:30pm Rm B
Chair: D. Hightower, GE Calma
Organizers: A. Dunlop, B. Preas, D. Schweikert
28.1 A Hierarchical Global Wiring Algorithm For Custom Chip Design
28.2 Algorithms for Global Routing J.G. Shone, UC Berkeley
28.3 A Channel Router For Non-Rectangular Channels in the Industrial Environment
C.H. Ng, VLSI Technology, Inc.

Session Number: 29, Hardware Design Languages
R 3:30-5:30pm Rm C
Chair: E. Clarke, CMU
Organizer: M. Barbacci
29.1 Flow Graph Representation D. Gajski, A. Orologiu, Unv. of Illinois at Urbana
29.2 A Design Rule Database System To Support Technology Adaptable Applications * H.J. Kahn, J.S. Aude, Univ. of Manchester
29.3 STL—A High Level Language for Simulation and Test J. Jive, K.-W. L. Lai, SDA Systems
29.4 GENERIC: A Silicon Compiler Support Language J.A. Solworth, Cornell Univ.

Session Number: 30, Tutorial: Built-in Self-Test
T 3:30-4:30pm Rm D
I. Sedmak, Self-Test Services

T 4:30-5:30pm Rm D
R. Joubbani, Tripler Technologies Corp.

Session Number: 32, Special Topics in Test Generation and Fault Simulation
R 8:00-10:00am Rm A
Chair: V. Agrawal, AT&T Bell Labs
Organizers: S. Dasgupta, P.W. Horstmann
32.1 On Fault Modeling For Dynamic MOS Circuits H.J. Wunderlich, W. Rosenstiel, Univ. of Karlsruhe
32.2 Effectiveness of Heuristic Measures For PODEM S. Patel, IBM Corp.; J. Patel, Univ. of Illinois at Urbana
32.3 Mixed Level Fault Coverage Estimation H.K. Ma, A. Sangiovanni-Vincentelli, UC Berkeley
32.4 Optimal Order Of The VLSI IC Testing Sequence W. Maly, CMU

Session Number: 33, Parallel CAD Hardware Accelerators
R 8:00-10:00am Rm B
Chair: T. Blank, Stanford Univ.
Organizer: R.A. Rutenbar, CMU
33.1 Multiprocessor-based Placement R.A. Rutenbar, S.A. Kravitz, CMU
33.2 A Parallel Adaptive Routing Algorithm And Its Implementation On A Two-Dimensional Array Processor T. Watanabe, Y. Sugiyama, NTT Electrical Communications Laboratories
33.3 HAL II; A Mixed Level Hardware Logic Simulation System S. Takasaki, T. Satani, N. Nomizu, H. Ishikura, N. Kóike, NEC Corp.
33.4 An Empirical Analysis of the Performance Of A Multi-Processor-Based Circuit Simulator * G.K. Jacob, A.R. Newton, D.O. Pederson, UC Berkeley

Session Number: 34, Expert Systems for Design Automation
R 8:00-10:00am Rm C
Chair: R. Joubbani, Tripler Technologies Corp.
Organizer: D. Gajski
34.1 A Rule-Based Logic Circuit Synthesis System for CMOS Gate Arrays T. Saito, H. Sugimoto, M. Yamazaki, N. Kawato, Fujitsu Labs Ltd.
34.2 FLUTE—A Floorplanning Agent For Full Custom VLSI Design H. Wantanabe, B. Ackland, AT&T Bell Labs
34.3 Knowledge-Based Optimal IIL Circuit Generator From Conventional Logic Descriptions T. Wantanabe, T. Masuiishi, Hitachi Systems Development; T. Nishiyama, Hitachi Microcomputer Eng., Ltd.; N. Horiuchi, Hitachi Tatsukawa Works
34.4 PEARL: An Expert System For Power Supply Layout E. DeJesus, Digital Equipment Corp.

Session Number: 35, Tutorial: Automatic Placement: A Review of Current Techniques T 8:00-9:00am Rm D
B.T. Preas, P.G. Karger, Xerox Palo Alto Research Ctr.

Session Number: 36, Panel: Floor Planning Systems P 9:00-10:00am Rm D
Chair: H. Rijkin, RCA
Panelists: W. Heller, IBM; H.-F. S. Law, SDA; D. Reiser, SDL; A. Sangiovanni-Vincentelli, UC-Berkeley

Session Number: 37, Regular Array Synthesis R 10:30-12:00pm Rm A
Chair: P. Agrawal, AT&T Bell Labs
Organizer: A. DeGeus
37.1 GENIE: A Generalized Array Optimizer for VLSI Synthesis S. Desudas, A.R. Newton, UC Berkeley
37.2 Comparisons of CMOS PLA and Polycell Representations of Control Logic C.M. Gerveshi, AT&T Bell Labs
37.3 Implementing FSM-to-PLA State Assignment Heuristics A. Coppola, Intel Corp.

Session Number: 38, Short Papers: Representing and Manipulating VLSI Design S 10:30-12:00pm Rm B
Chair: J.B. Rosenberg, MCNC
Organizer: R.A. Rutenbar
38.1 Escher—A Geometrical Layout System For Recursively Defined Circuits E.M. Clarke, Y. Feng, CMU
38.2 MADMACS; A New VLSI Layout Macro Editor P. Frano, E. Gautrin, IRISA Campus De Beaulieu, France
38.3 A Specification Language For Describing Rectilinear Steiner Tree Configurations A. P.-C. Ng, P. Raghavan, C.D. Thompson, UC Berkeley
38.4 Dual Quadtree Representation for VLSI Designs I.V. Ramakrishnan, S.K. Nandy, SUNY at Stony Brook
38.5 Precedent Based Reasoning About VLSI Structures R.H. Lathrop, MIT AI Lab; R.S. Kirks, Gould AMI Semiconductors
38.6 A Frame Based System For Representing Knowledge About VLSI Design H.K. Reiehn, W.S. Adolph, A. Sannugamadura, Simon Fraser Univ.

Session Number: 39, Timing Verification (1) R 10:30-12:00pm Rm C
Chair: J.L. Rivero, IBM Corp.
39.1 A Rule Based Approach to Unifying Functional and Fault Simulation and Timing Verification S. Ghosh, AT&T Bell Labs.
39.3 Delay Reduction Using Simulated Annealing J.D. Finchus, A. Despain, UC Berkeley

Session Number: 40, Printed Circuit Board (PCB) Routing (1) R 10:30-12:00pm Rm D
Chair: P.S. Hostiger, IBM Corp.
Organizer: R.B. Hitchcock
40.1 A New Approach To Multi-Layer PCB Routing H.C. Du, J.F. Naveda, K.C. Chang, Univ. of Minnesota
40.2 A Preprocessor For Layer Assignment Problem H.C. Du, K.C. Chang, Univ. of Minnesota
40.3 Near Optimal n-Layer Channel Routing H.C. Du, R.J. Enbody, Univ. of Minnesota

Session Number: 41, Silicon Compilation R 1:30-3:00pm Rm A
Chair: J. Fox, GTE Labs
Organizer: D. Gajski
41.1 Principles Of The Syco Compiler A. Jerraya, R. Jamier, B. Courtois, TIM3-Image/INPG, France
41.2 DATAPATH: A CMOS Datapath Silicon Assembler T. Marshburn, R. Brown, J. Lui, D. Cheung, G. Lum, P. Cheng, Hewlett-Packard
41.3 An Intelligent Module Generator Environment P. Six, L. Claesen, J. Rabaey, H. De Man, IMEC—VSDM Division, Belgium
41.4 HAPPI; A Chip Compiler Based On Double Level Metal Technology R. Pianatuma, D. Smith, S. McNeary, J. Crabbe, RCA Corp.

Session Number: 42, Database II R 1:30-3:00pm Rm B
Chair: R. Katz, UC Berkeley
Organizer: N. Elias
42.1 An Object Oriented, Procedural Database For VLSI Chip Planning W. Wolf, AT&T Bell Labs
42.2 An Automated Database Design Tool Using The ELKA Conceptual Model M.C.J. Sautesta, Inst. de Investigaciones Elec., Mexico; A.P. Buchmann, National Univ. of Mexico
42.3 A Database Interface For An Integrated CAD System C. Jullien, A. LeBlond, Centre National d’Etudes des Telecommunications, France
42.4 Rules-Based Object Clustering: A Data Structure For Symbolic VLSI Synthesis And Analysis R.P. Larsen, Rockwell International Corp.

Session Number: 43, Timing Verification (3) R 1:30-3:00pm Rm C
Chair: J.L. Rivero, IBM Corp.
43.1 Simulating and Controlling the Effects of Transmission Line Impedance Mismatches R.E. Carriaght, Martin Marietta Orlando Aerospace
43.2 A Delay Test System For High Speed Logic LSIs K. Kishida, F. Shirotori, Y. Ikemoto, S. Ishiyama, T. Hayashi, Hitachi Ltd.
43.3 Panel: Future Directions in Timing Verification

Session Number: 44, Printed Circuit Board (PCB) Routing (2) R 1:30-3:00pm Rm D
Chair: P.S. Hostiger, IBM Corp.
44.1 Router System For Printed Wiring Boards Of Very High Speed, Very Large-Scale Computers * T. Tada, A. Hanafusa, Fujiitsu Ltd.
44.2 Global Forced Hierarchical Router J. Kessenech, G. Jackoway, Hewlett-Packard
44.3 Hierarchical Dynamic Power K. Kawamura, H. Shiraiishi, M. Umeda, Fujitsu Laboratories Ltd.
44.4 A Parameter Driven Router * J.W. Smith, V.S. Bobba, Univ. of Georgia