The VHSIC Hardware Description Language – A Glimpse of the Future

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This issue of Design & Test provides a basis for understanding the new hardware design and description language being developed under the auspices of the Department of Defense’s Very-High-Speed Integrated Circuits (VHSIC) Program. The language is popularly known by the acronym VHDL, which stands for VHSIC Hardware Description Language. It employs structures of building blocks to describe complex VLSI designs in terms of abstract architectural concepts, all in an integrated, descriptive unit.

The language allows the user to separate control from dataflows; differentiate between memoried and combinatorial elements; create user-defined types; and describe a design hierarchically, thus facilitating the design process. Other excellent hardware description languages in industry today cover various aspects of hardware design and description, but none matches VHDL’s total capabilities.

The six articles in this issue were selected to give the reader a general understanding of VHDL from several points of view. Each author was either a direct contributor to the government contract, a consultant during the development work, or a progenitor of the VHDL concept; some authors played multiple roles. All believe in the value of VHDL and want to improve it through language extensions. This common desire is especially clear in the critique of VHDL.

The first article, "VHDL Motivation," by Allen Dewey and Anthony Gadient, explains the many reasons for a standard design and description language. The motivation came from the Department of Defense, but the need is universal. The authors discuss the elements motivating HDL use, particularly VHDL, and examine VHDL’s potential impact on government, academic, and industrial participation in electronic research, education, and business. The authors certainly understand these motivations; Dewey was government contracting officer throughout the proposal phase, as well as for much of the implementation phase of the language and support environment from mid-1982 through August 1985. Gadient is intimately involved with the DoD VHSIC program. The article sets the stage for those that follow.
One of the tasks in developing a new language is stating the language requirements. This process requires analyzing existing languages to ensure that features which have already been found useful and necessary are not overlooked in the process of generating new hardware description language requirements. During the VHDL effort, detailed language requirements were thoroughly defined. The second article, "VHDL: Feature Description and Analysis," by Jim Aylor, Ron Waxman, and Charlie Scarratt, uses the results of that study, plus analyses of other languages, to compare the coverage of the required features by VHDL and eight other languages. The authors were intimately involved in generating requirements and analyses during the contract.

"VHDL—The Language," by Roger Lipsett, Erich Marschner, and Moe Shahdad, "discusses elements of the VHDL language and their use in modeling various aspects of hardware." This article provides a comprehensive view of the language's organization and salient features, and discusses hardware abstraction and its application to hierarchical hardware-modeling techniques. VHDL's capabilities are illustrated by using a comprehensive VHDL description which is thoroughly explained in the text. The authors are the key language designers for VHDL.

A hardware description language is only useful if it includes a suitable support environment. Alfred Gilman's article, "VHDL—The Designer Environment," describes the VHDL support environment as "an open-ended integration framework" with a toolset that enables design and documentation. The support environment is composed of a design library and five tools: Analyzer, Reverse Analyzer, Design Library Manager, Simplifier, and Simulator. These tools are being developed by many tool designers in the VHDL development team. The author is the system architect for creating an open-ended "system" that both integrates the existing VHDL toolset and easily accepts other tools as they become available.

Although hardware test was not addressed directly within the VHDL contract, the principles of hardware design and description subsume the ability to describe a model of a unit under test. "VHDL's Impact On Test," by Al Lowenstein and Greg Winter, discusses how VHDL can be used within the test environment. The authors present examples of VHDL descriptions and relate them to the particular area of the test environment in which they are useful. The article points out the need for a standard hardware description language that spans the lifecycle of a hardware component—design, test, manufacturing, and maintenance. The authors are still involved in applying VHDL to the hardware test and tester environment.

While the tone of this issue is complimentary to VHDL, all developments can stand some criticism. The article by Dan Nash and Larry Saunders, "A VHDL Critique," presents both positive and negative criticism of VHDL. The authors note that some aspects of VHDL are acknowledged as good, others as deficient, and still others as controversial. They discuss each of these categories and offer some criticism related to the limitations imposed on VHDL by the VHDL contract. They conclude that VHDL represents a significant advance in state-of-the-art hardware description languages and that it "may very well be considered ...the first generally accepted standard language." Dan Nash contributed to the original Wood's Hole document which provided the first statement of VHDL requirements. He has also been a consultant to the government on VHDL development. Larry Saunders has acted as a consultant to the VHDL design team.

VHDL provides a foundation for the communities of design automation, design and test, and manufacturing to reduce product cost through improved designer productivity and maintenance capabilities. A standard machine-readable description of design data will enable developers of design workstations, test equipment, and design automation software to provide common data interfaces among their tools. This capability will lead to an expanded array of useful products for hardware design and test. In addition, VHDL will promote efficient machine-to-machine communication of data among participating organizations. Such machine-to-machine communication will enable easy reuse of off-the-shelf hardware products.

Designers will also be able to use design analysis tools to evaluate existing hardware products for use in new applications. Standard human-readable descriptions of design data will facilitate exchange of that data among designers, enabling them to work effectively with design tools. VHDL's special features make it suitable not only as a descriptive medium, but also as a design tool. Thus, VHDL provides a glimpse of a future which will see a giant step forward in the realm of VLSI design and test, just when such a step is imperative.

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