Analysts forecast end of semiconductor slump

The worst recession in the semiconductor industry's history will bottom out late this year, returning to substantial growth in 1987, analysts predict.

Speaking during the Semiconductor Equipment and Materials Institute's ninth annual Information Services Seminar in Newport Beach, California, 13 analysts presented their forecasts for 1986 and beyond.

Jack Beedle, president of In-Stat, Inc., predicted that total dollar sales in the US semiconductor industry will drop 3.7 percent this year. The book-to-bill ratio, he noted, will climb to 1.00 during the first quarter, continuing to climb steadily and reaching 1.15 by the fourth quarter. Beedle cautioned, however, that his forecasts were based on the OEM market remaining strong.

John Lazlo, Jr., vice-president of Morgan Stanley and Company, predicted a slow upturn, with final figures showing 1986 as a "break-even year."

Thomas Kurlak, vice-president of Merrill Lynch, called 1986 a "gradual recovery year," with a restructuring of the global semiconductor industry shifting emphasis from capital intensity to design-intensive or ASIC markets.

In the materials area, Daniel Rose, president of Rose Associates, forecast a four percent rise after the disastrous 40 percent slide of 1985. He sees 1987 as a "barn-burner year," however, with a 45 percent growth in the materials industry.

Japanese materials suppliers captured an unprecedented 51 percent of the world materials market in 1985, Rose reported, a feat that he attributed to a major "quality gap" between US and Japanese products.

Rose also foresees a major shake-out of the world's silicon wafer suppliers during the next few years: At current production rates, he noted, there will be a 75 percent overcapacity in silicon wafers by 1988.

While concurring with projections for Semiconductor Industry upswings, Jerry Hutcheson, president and CEO of VLSI Research, Inc., warned against overextended hopes for the ASIC market. He anticipates a drop in that market in a few years, much like the decline in DRAMs.

Hutcheson expects a shift in the test equipment market, with reliance on final test decreasing in favor of probe testing. The industry, he said, is moving toward contactless probing, and future fabrication lines will merge E-beam lithography and E-beam testing.

Citing the semiconductor industry's historic pattern of two "down-years" followed by one boom "up-year," economist A. Gary Shilling warned that the current cycle, which began in 1984, broke the pattern with unprecedented growth in the first year followed by a depressed second year.

Noting that 1986 should therefore be the final down-year in the current cycle, Shilling cautioned that if the next cycle picks up the historic pattern, the industry may be faced with a prolonged down cycle lasting until 1989.

Test Technology Newsletter merges with D&T

Effective with the appointment of its former editor to the D&T Editorial Board, the IEEE Test Technology Newsletter has merged with D&T.

Edited for three years by Marc Harrison, the quarterly newsletter included test-related news, reports, and articles, as well as periodic guest columns. Those topics will now be incorporated into D&T Scene and other departments of the magazine, including Conferences, New Products, Research, Standards, and Book Reviews.

"I'm excited to be reaching a larger and more diverse audience," Harrison noted. "I look forward to serving the readers of IEEE Design & Test. I see Scene as a two-way street, and I'm anxious to receive suggestions and input from readers."

SEMI begins data collection program

The Semiconductor Equipment and Materials Institute has begun an industry-wide data collection program to track worldwide sales of semiconductor manufacturing equipment and materials.

The program will provide industry statistics on monthly sales, bookings, and backlog orders for front-end processing equipment, back-end equipment, and materials. Categorical reports will be further broken down by geographic region to provide dollar totals for the North American, Japanese, European, and rest-of-world markets, according to a spokesperson.

Any firm that manufactures semiconductor processing equipment or materials can participate in the program. A professional accounting firm will accept reports from participants to ensure confidentiality.

Further information on the program is available from Ron Jacob, data collection manager, SEMI, 625 Ellis St., Suite 212, Mountain View, CA 94043.
Harrison named new Scene editor

Marc L. Harrison has been named to the D&T Editorial Board as editor of D&T Scene, replacing Gordon Padwick, who held the post since the magazine’s inception.

Harrison is a microprocessor technical consultant at AT&T Information Systems, Holmdel, New Jersey. He is responsible for supporting users of AT&T’s UNIX Microsystem. Previously, he was involved in the design of AT&T WE 32100 microprocessor. He has been with AT&T since 1978.

Harrison was editor of the IEEE Test Technology Newsletter from 1983 until this year (see related article in this issue). He was president of the IEEE chapter at SUNY Stony Brook from 1976-1978.

Harrison received his BE and MS degrees in electrical engineering from SUNY at Stony Brook in 1978. He is a member of Tau Beta Pi and Eta Kappa Nu.

Fujiwara joins D&T Editorial Board

Hideo Fujiwara, inventor of the FAN algorithm for automatic test generation, has joined the D&T Editorial Board as a Far East Editor.

Fujiwara, an associate professor in the Department of Electronics and Communications at Meiji University, Tokyo, has been with the Department of Electronic Engineering at Osaka University since 1974. He was a visiting research assistant professor at the University of Waterloo, and a visiting associate professor at McGill University, Montreal.

His research interests include logic design, design for testability, test pattern generation, fault simulation, built-in self-test, and expert systems for design and test. He is the author of Logic Testing and Design for Testability.

Fujiwara received the BE, ME, and PhD degrees in electronic engineering from Osaka University in 1969, 1971, and 1974, respectively. He is a senior member of the IEEE as well as a member of the Institute of Electronics and Communication Engineers of Japan and the Information Processing Society of Japan. He received the IEEE Young Engineer Award in 1977.

Erratum

In the December 1985 issue of D&T, several pages of “PROD: A VLSI Fault Diagnosis System,” by Peter Odryna and Andrzej Strojwas, were printed out of sequence. The pages numbered 33 and 34 should appear ahead of those numbered 31 and 32.

Kilby honored by IEEE

Jack St. Clair Kilby, a pioneer in the development of the monolithic IC, recently received the 1986 Medal of Honor from the IEEE.

Kilby, an independent consultant and inventor based in Dallas, holds more than 50 patents, including several covering the monolithic IC that laid the conceptual and technological foundation for the entire field of integrated electronics.

Kilby received the BS and MS degrees from the University of Illinois and the University of Wisconsin, respectively. In 1947, he joined the CentraLab Division of Globe Union, Inc., where he spent 11 years in the design and development of semiconductor devices with ceramic-based, silk-screened circuits. He joined Texas Instruments, Inc., in 1958, serving as engineer, entrepreneur, and administrator until taking a leave of absence to become a consultant in 1970.

He is a Fellow of the IEEE and a member of the National Academy of Engineering and Eta Kappa Nu. He has received numerous awards for his scientific achievements.

About the cover

This month’s cover uses a Mobius strip to illustrate the synthesis—and resultant blurring of distinctions—between the machine-readable VHDL and the hardware it describes. As the language conveys a description of one machine to another, it becomes in effect a part of the hardware in which it is used. Ideally, VHDL will provide a standard that can be used by design and test professionals alike, facilitating the synthesis of the two fields.

The Mobius strip allows us to follow the flow from machine to language and back to hardware; although the loop appears to have two sides, it really has only one. Skeptical? Try it: take a strip of paper, give it a 180-degree half twist, and glue or tape the ends together to make a loop. Now place a pencil point on the strip and draw a line all the way around, never lifting the pencil from the paper. You'll soon return to your starting point, and the line will appear on both “sides” of the loop!