Sampling Quality

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This special issue had its genesis in the 22nd Design Automation Conference, held June 23-26, 1985, in Las Vegas. Of the 125 high-quality papers presented at that meeting, seven were eventually selected, updated, and augmented as representative of the areas covered. There are four articles from universities and three from industry covering the areas of layout, silicon compilation with testability, design rule checking and layout analysis, computer-aided manufacturing, and automated schematic entry. Many of the articles in this issue emphasize not only design automation, but obtaining solutions to problems that require the human designer to provide the intelligence for producing results superior to those obtained by automation alone.

The attempt to incorporate testability features in a silicon compiler is a healthy one. Silicon compilation with the usual metrics of automated synthesis, and without testability considerations, can produce results that are difficult to test. With this introduction, let us look at the seven articles:

"WEAVER: A Knowledge-Based Routing Expert," by Rostam Joobbani and Daniel Siewiorek of Carnegie-Mellon University, describes a channel/switchbox routing program that uses some of the concepts in artificial intelligence. The authors demonstrate through various examples that their knowledge-based approach is a practical means of solving the knowledge-intensive problem of VLSI chip routing. They claim that such an approach improves the quality of the final layout by considering a large number of often conflicting metrics. WEAVER does away with the restriction of using strictly vertical lines on different layers. Examples provide a comparison with other routing techniques.

The article, "Magic’s Circuit Extractor," by Walter Scott and John Ousterhout, addresses a very important and crucial tool in any VLSI design methodology: circuit extraction. The extractor is part of the Magic VLSI layout system developed at the University of California, Berkeley, and described in the February 1985 issue of D&T. Magic’s extractor, which is hierarchical and incremental, is also both practical and efficient. The extractor is based on a new algorithm called corner-stitching, and is applicable for various MOS technologies. The authors compare their extractor favorably with several others using the metric of number of FETs extracted per second.

"The CMU-CAM System," by Andrzej Strojwas, describes a software system being developed at Carnegie-Mellon University which has several applications in the area of process design and fabrication of VLSI chips. The components of this CAM system are described with special attention to the computational efficiency of the algorithms, also developed at CMU. The author stresses the importance of integrating the software for the three main steps in a VLSI chip design—system/circuit design, fabrication process design, and manufacturing control.

The next article, "An Automatic DFT System for the Silc Silicon Compiler," by H.S. Fung and Sanford Hirschhorn, examines the incorporation of design for testability into a silicon compiler now under development at GTE Laboratories. The DFT approaches chosen combine built-in self-test and scan path. The system uses a
testability expert that accumulates testability knowledge and makes the important testability decisions during the synthesis procedure. The article also provides a very comprehensive bibliography on test generation, testability analysis, and design for testability.

Automating the difficult and tedious task of generating schematic diagrams from connectivity descriptions is discussed in "Automatic Generation of Digital System Schematic Diagrams," by Anshul Kumar, Anjali Arya, V.V. Swaminathan, and Amit Misra of the Indian Institute of Technology, New Delhi. This problem is partitioned into several steps, considering the steps that a human designer would take, and an efficient solution is found for each step, making suitable approximations. Examples illustrate each step in the methodology.

The article, "Hierarchical Analysis of IC Artwork with User-Defined Abstraction Rules," by Louis Scheffer and Ronny Soetarman, describes a hierarchical design rule checker and a layout extractor. The authors cite those infrequent cases where hierarchical analysis is not practical, noting that such cases are candidates for automatic handling. The added flexibility in the system is also cited among the practical advantages of providing hierarchical analysis. The authors demonstrate this by using several full custom chips as examples.

"The VIVID Symbolic Design System: Current Overview and Future Directions," by Durward Rogers, describes the various components of the VIVID system from the Microelectronics Center of North Carolina. These components include tools for symbolic virtual-grid layout, layout verification, and hierarchical compaction. The tools were selected based on the feedback from both academic and industrial designers of the original VIVID system that was released about a year ago. The article describes evolutionary plans for CAD tool system development at MCNC to accommodate larger and more complex VLSI chips.

For this special issue, we encouraged authors of 25 papers from the Design Automation Conference to submit manuscripts. The authors were informed that their article would go through the normal D&T review procedure. Further, it was made clear that acceptance of the article was strongly dependent on the submission of an enhanced version representing a significant improvement over the one that was presented at the DAC. Each article was reviewed by three referees, with the final seven selected on the basis of their recommendations. Putting together this issue involved the cooperation of about 35 reviewers, each of whom received no more than two articles.

My sincere thanks go to each of the reviewers for a job superbly and professionally done. I would also like to express my appreciation to Roy Russo, former editor-in-chief of this magazine, and to Larry O'Neill, program committee chairman of the 1985 DAC, for giving me the opportunity to serve as guest editor. Also, I would like to thank Vishwani D. Agrawal, editor-in-chief, for his guidance throughout this issue. Last but not the least, I would like to express my thanks to Mickey Schach, managing editor, for superbly coordinating the publication of this issue on time.

Prathima Agrawal received the B.E. and M.E. degrees (with distinction) in electrical communication engineering from the Indian Institute of Science, Bangalore, India, and the PhD in electrical engineering from the University of Southern California. She has been with AT&T Bell Laboratories since 1978, and currently is a member of the technical staff at Bell Labs' Computer Technology Research Laboratory, Murray Hill, N.J., working on logic minimization, test generation, partitioning algorithms for hardware accelerators, and fault-tolerant computing. Prior to joining AT&T Bell Labs, she worked on problems of test generation and automatic routing, and in 1977 served as an assistant professor of electrical engineering at California State University, Northridge.

Agrawal received AT&T Bell Labs' Distinguished MTS award in 1985. She has been a member of the Technical Program Committee of the DAC since 1982. She served as vice chairperson for CAD on the Technical Program Committee of the IEEE ICCD '85, and currently chairs the architecture and algorithms sections of the committee for ICCD '86. Agrawal is a senior member of the IEEE.