ICOT leader Moto-oka dies

Tohru Moto-oka

Professor Tohru Moto-oka, a leader in Japan’s Fifth-Generation Computer Project and director of the computer center at the University of Tokyo, died of cancer on November 11, 1985. He was 56 years old.

Moto-oka was the subject of an interview on the Fifth-Generation Computer Systems Project in the October 1985 issue of D&T. A leader in the fields of computer architecture and design automation in Japan, he was born in Tokyo and received his Bachelor of Engineering in electrical engineering in 1952 and his Doctor of Engineering in electrical engineering in 1958, both from the University of Tokyo. Moto-oka joined the Faculty of Engineering at the University in 1957 and continued in that capacity until his death.

He was also a visiting research assistant professor at the University of Illinois and a visiting professor at Washington University in St. Louis. As chairman of the Fifth-Generation Computer Project’s promotion committee, Moto-oka was instrumental in developing its direction. He organized and chaired two International Conferences on Fifth-Generation Computer Systems, FGCS ‘81 and FGCS ‘84. He also was active in the Japanese National Project of Scientific Super Computers, the Japanese National Committee of ISO TC 97/SC 21, and in the DA working groups of the Institute of Electrical Engineers of Japan and the Information Processing Society of Japan.

In addition, he chaired the DA Survey Committee of the Japan Electric Industry Development Association, and in 1975 served as general chairman of the first US-Japan DA Symposium. Moto-oka was also active as general chairman of ICTP ‘83, IEEE/IFIP CHDL ‘85, and IFIP VLSI ‘85. His research included the fields of computer architecture, distributed computer systems, inference machines, database machines, parallel processing, computer-aided logic design systems, and artificial intelligence.

Moto-oka was posthumously awarded the Zuihosho, the Order of the Sacred Treasure from the Emperor of Japan, on December 6, 1985.

SUPER, STAR predict design reliability

Two automated reliability engineering systems developed by AT&T Bell Laboratories predict product design reliability before a prototype is constructed, and forecast the product’s future reliability based on early experience.

Intended for internal use by AT&T Bell Labs, both systems run on the Unix operating system; they combine quality assurance and probability theory with statistics and computer programming to predict reliability and allow designers to pinpoint problems early.

The System Used for Prediction and Evaluation of Reliability, or SUPER, “acts like a high-tech crystal ball in the early design stage” to predict how well a computerized blueprint will perform as an actual product, a spokesperson said. Later, the Statistical Analysis of Reliability, or STAR, system analyzes reliability data from accelerated life tests and field trials.

Although SUPER generally uses the reliability history of the parts called for in a product’s design to forecast reliability, it can also deal with parts too new to have a quality history, the company claims. In such situations, the system asks for information concerning the part’s underlying technology and, using a database having the history of microprocessors with similar characteristics, makes “an educated guess” about reliability, the spokesperson noted.

AT&T to provide worldwide circuit design capability

Along with opening the company’s first domestic application-specific IC design center in Sunnyvale, California, AT&T has revealed that it is also operating an ASIC design center in Munich, West Germany, and is considering additional design centers in the US and abroad.

The centers will be available for worldwide use, allowing microchip designers to create and produce high-quality ASICs without special knowledge of device physics or silicon design, according to the firm. Rather than focusing on layout, the designer can concentrate on the functions the chip must perform for the system.

The design automation system includes sophisticated CAD tools and libraries developed by AT&T Bell Laboratories, and is the result of more than 12 years of technological evolution.

Customers can elect to use the AT&T DA system themselves or have the work performed by AT&T staff designers. “We’re offering our customers around the world the opportunity to access our Da system,” said John M. Nemecek, executive vice-president of AT&T’s Components and Electronic Systems Division.

Clients will be able to take advantage of the company’s development experience in designing more than a thousand custom ICs; AT&T’s current prototype success rate exceeds 95 percent, according to a spokesperson.

In addition, customers can draw from AT&T’s extensive experience in CMOS processing technology, and they will have access to a full range of AT&T assembly and testing services.

The design system is based on a standard-cell approach. Once a custom design has been created, it can be transmitted within seconds, via computer, to one of AT&T’s seven IC manufacturing plants. There, computers can immediately begin generating specifications and manufacturing instructions for full-scale chip production.
Massachusetts Microelectronic Center established

Industry, higher education and government have banded together in Massachusetts to establish an educational center dedicated to VLSI chip technology.

The Massachusetts Microelectronic Center, Westborough, was formed to answer the state's need for highly trained professionals to work for its numerous computer manufacturers.

Although universities and university consortia had plenty of interested students, the programs lacked funds and faculty necessary for specialized training; businesses, however, possessed the equipment and the know-how, but neither students nor formal training capabilities.

The legal structure and seed money necessary to launch the project were provided by the state legislature, which agreed to provide $20 million in start-up costs, provided the figure was matched by industry through in-kind contributions of technical equipment and cash. The legislature will also provide a continuing operating budget while industry continues its contributions of cash and updated equipment.


Nine universities, in turn, agreed to contribute faculty, formal educational programs, classroom and laboratory space, and students. Participating institutions are the Southeastern Massachusetts University, Worcester Polytechnic Institute, University of Lowell, Merrimack College, University of Massachusetts (Amherst), Boston University, Tufts University, Northeastern University, and the Massachusetts Institute of Technology.

Start-up and operations of the Center are being directed by the Massachusetts Technology Park Corporation, established by the legislature to develop the project. The corporation is composed of Executive Director Joseph Stach and a compact staff, carrying out the instructions of a 23-member board of directors.

Following initial evaluation, the board concluded that the primary need was a method for training students in microcircuit design. The Center was in turn designed in a three-part configuration consisting of a VLSI CAD Network, already operating in rented space with a half-dozen graduate students participating—an IC Fabrication Facility, and a Semiconductor Instructional Process Laboratory.

The CAD Network will be based at the heart of the 36-acre campus in Westborough, connected with CAD modules in seven university locations around the state. Depending on the student load anticipated, each institution will eventually be provided with from one to eight student modules, each capable of supporting 15 to 20 students per semester.

Hardware will consist of a processor—typically a 32-bit super-minicomputer—with a capacity of about two million instructions per second; 16M bytes of memory; 600-800M bytes of disk storage, an operator's console; and a 1600/6250 BPI tape drive. Four alphanumeric terminals, four color graphics terminals, and at least one line printer, plotter, and 9600-Baud modem will also be included.

System software, to be updated as needed, will include a Unix 4.2-compatible operating system and various CAD tools, including a layout editor, display program, design rule checker, simulator, and circuit analysis program.

The Integrated Circuit Fabrication Facility will be specially constructed to boost turnaround time from submission of a design to delivery of a packaged chip. Whereas proprietary fabrication facilities require from 11 to 14 weeks turnaround time, the ICFF will be approximately four weeks. The ICFF is expected to turn out approximately 2500 student circuits per year.

Student design data received over the CAD Network will be processed through the four major operational areas of the facility: photomask, fabrication, testing, and assembly. The product produced will be a packaged IC that the student can subject to electrical characterization and performance evaluation.

The Semiconductor Instructional Process Laboratory will provide students with hands-on laboratory instructional experience. SIPL will have two components: a Central Semiconductor Instructional Process Laboratory located at the Center, and four Distributed Semiconductor Instructional Process Laboratories located on the campuses of participating universities.

Rehabilitation of six existing buildings on the old Lyman School site that will house the Center is proceeding. A new building will be constructed for the Integrated Circuit Fabrication Facility; this new structure will also house the Central Semiconductor Instructional Process Laboratory, with existing buildings to be used for the CAD Center, offices, laboratories, classrooms, and dormitories.

SEMI offers IC processing poster

A full-color poster depicting the major steps in the making of an integrated circuit is available from the Semiconductor Materials and Equipment Institute. "The Making of an Integrated Circuit" is a 24" × 36" poster featuring 20 detailed cutaway illustrations of the processing equipment and materials used in semiconductor manufacturing. Each illustration is accompanied by a brief caption explaining the equipment's function.

Detailed drawings depict crystal pulling, crystal slicing, lapping and polishing, an epitaxial reactor, pattern design, pattern generation, an oxidation furnace, photoresist coating, a wafer stepper, developing and baking, dry etching, an ion implanter, oxide deposition, metal deposition, wafer probing, dicing, die attach, wire bonding, encapsulation, and final testing.

The poster was illustrated by technical fine artist David Kimble. Technical assistance was provided by industry authorities Klaus Schuegraf of Tylan Corp., industry consultant Ben Yano, and the staff of TRW Semiconductor.

Cost for the poster is $25, with a limited number of special editions, signed by the artist, available for $50 each. To order, send a check payable to SEMI to SEMI, "Making of an IC" Poster, Dept. 05607, San Francisco, CA 94139; (415) 964-5111.
SEMI uptime document passes industry ballot

Suppliers and users of semiconductor processing equipment have ended years of industry debate by agreeing upon commonly accepted definitions of productive “uptime” included in a new document from the Semiconductor Equipment and Materials Institute, Inc.

The “Equipment-Dependent Uptime Document,” a product of the SEMI Standards Program, includes definitions of both “uptime” and “downtime” conditions as well as a formula for determining equipment-dependent uptime. The new document isolates the equipment from human factors, according to a spokesperson. Human factors are instead considered in a second document, “Comprehensive Uptime,” now under review by the organization’s Equipment Reliability Task Force.

In the past, differing perspectives led some manufacturers to treat setup as uptime, since it is part of the processing routine, while others considered it downtime because the equipment was not available for manufacturing product. Under the new standard, machinery setup time falls under “scheduled downtime.”

“We felt it was imperative to get vendors and users of equipment to use the same terminology...” a spokesperson said. “Without a standard formula, you’d ask five people for an uptime figure and get five different answers.”

Calay suggests benchmark standards

Citing the need for “standards of credibility” in the CAD industry, Calay Systems, Inc. has composed a list of 10 questions that prospective customers should ask before a vendor runs a benchmark of a CAD system for PC board design.

Using the benchmark as an effective evaluation tool requires that the customer bring the vendor a board that has already been designed by hand or using a competing CAD system, a spokesperson said.

Design time must have been carefully documented, because that time and the ease of use of the customer’s system form the benchmark for comparison against the vendor’s system. The vendor’s system is used to redesign the board and the new time compared to the previous design time to determine if the vendor’s system is faster and easier to use.

“There is no industry standard for benchmarks and there is not likely to be one unless customers demand it,” said Richard Finn, president and chief executive officer of Calay. Finn cited 10 questions developed by his firm to help customers ensure that what they see is what they will get.

1. Is the benchmark being run on a board previously designed in-house and carefully documented?
2. Is the CAD vendor asking for data on the board prior to the benchmark?
3. Is the vendor trying to restrict the complexity of the board to be benchmarked?
4. Is the system used for the benchmark configured the same way as the system you plan to buy, and does it use the same computer power as the one you will get as a result of the benchmark?
5. Will you be present for all phases of the benchmark?
6. Who will document the benchmark?
7. Can you submit engineering change orders during the benchmark?
8. Can you stay until the benchmark is completed?
9. Are your standards consistent?
10. Is the vendor asking you to pay for the benchmark?

Additional details are available from Calay Systems, Inc., 2698 White Road, Irvine, CA 92714: (714) 863-1700.

TI announces distribution program for semicustom ICs

Texas Instruments has announced a distributor program for marketing and design support of its application-specific IC products.

The new program allows TI’s distributors to work directly with their customers on the design of TI standard cell and gate array ICs. The program is intended to give potential users new design interface options as well as substantially increase the number of available ASIC design locations.

Adding TI’s ASIC products to the distributors’ lines will make available to the distributors’ customers TI’s complete line of digital logic alternatives, according to a spokesperson. These products range from the TTL and LS family to the newer AS/ALS, HCMOS and IMPACT PAL families, as well as the higher-integration ASIC options.

Distributors will initially market TI’s SN54/74SC library of three-micrometer CMOS standard cells, and 2.8-micrometer TAC H and 2.3-micrometer VH series CMOS gate arrays, second-sourced by Philips/Signetics and Fujitsu, respectively. This product offering meets or exceeds HCMOS specifications and offers the same advantages of low power consumption, high noise immunity, and switching speeds comparable to low-power Schottky performance. The library currently contains more than 200 SSI, MSI, I/O, and complex cells.

The first TI authorized distributor participating in the ASIC program is Wyle Laboratories, with participation by Arrow Electronics and others to be announced. Wyle will support customers through its regional design centers in Santa Clara and Irvine, California, and Denver, Colorado.

The design centers feature Daisy design system workstations, onto which TI will load and support its standard cell and gate array libraries. Each library contains all necessary software files: schematic drawings for cells; corresponding simulation models, including capacitive loading comprehension; and a netlist output file that is automatically converted to TI’s design languages. The software will enable distributor design center engineers and/or customers to implement front-end logic design, simulation, and debug phases independently, the spokesperson noted.

When the customer’s design has been implemented and verified, a design specification will be released form the distributor to TI. The specification will be verified by TI and will become the controlling document for all subsequent steps in the prototype development cycle.

TI plans to expand the ASIC program with a broad range of design support alternatives for customers to include TI’s seven Regional Design Technology Centers located in Atlanta, Chicago, Dallas, Northern and Southern California, and Canada; authorized ASIC distributors; and free libraries for popular engineering workstations and PC-based design systems.
SRC’s role in semiconductor industry transition

The transition now occurring in the semiconductor industry points out the need for US companies to rethink their attitudes in order to remain competitive, according to Larry W. Sumney, president of Semiconductor Research Corporation.

In a recent issue of the SRC Newsletter, Sumney cited the ever-increasing rate of change in information technology and the merging of the four-tier structure of materials, components, equipment, and systems into a one- or two-tier continuum among the evidence that the current industry structure may be radically different following the next industry downturn.

Noting that US firms have traditionally declined to share data that they considered proprietary, Sumney indicated that such sharing in other nations has allowed foreign companies to advance rapidly, threatening US leadership in the industry.

High domestic labor costs, lack of funding for university programs, and limited funds for R&D have also contributed to the problem.

“Something has to change in the United States if we are to continue leadership in ICs, with all of the implications of this leadership, as the world moves toward an information-based economy,” he wrote.

That change is SRC’s goal—one the organization hopes to achieve, in part, through expanding its role as a cooperative research mechanism. University participation is providing an increasing flow of information that is being passed along to the more than 60 companies affiliated with the SRC. Such research provides both well-trained graduates and a variety of short-term products.

Results from SRC research are immediately available to members and in time become generally available, according to Sumney. If other information can be shared as well, the SRC could act as a catalyst, also providing both the repository and distribution system.

Another possible role is knowledge enhancement: enabling the more efficient use of existing information, he noted. This goal could be accomplished by establishing both general and specific databases even more powerful than those now maintained by the organization. Such an undertaking, he warned, would challenge system architects working on the organization and retrieval strategy.

The SRC could also provide member forums for technology assessment or for discussion of issues facing the industry, Sumney wrote. The organization has already organized a technology assessment meeting that examined the status of three current technical areas. In a separate project, mutual interests in manufacturing tools are being discussed in order to identify recommendations to members concerning actions designed to benefit both them and the US industry.

Such new roles, the president noted, are complementary to those already being played by existing organizations serving the semiconductor industry.

“As the semiconductor industry develops toward the $100 billion markets of the future, there is little doubt that substantial changes will be occurring,” Sumney wrote. “The SRC expects to mature in its activities and to be a major contributor to the industry and to the maintenance of a strong competitive position for its members in this industry. Our inexorable conviction is that the continued success of this industry is key to the success of the United States as we move into the information age.”

Honeywell opens Microtechnology Center

Honeywell has opened a new Microtechnology Center that will specialize in using VHSC-level technology to design products for large-scale logic systems. The Center, an operation of Honeywell’s Solid State Electronics Division, initially will employ about 40 people. Robert M. Sullivan has been named director.

The new facility is located in Phoenix, Arizona, to take advantage of the broad systems knowledge and skills developed in the parent firm’s Phoenix-based Large Systems Division, according to a spokesperson.

Services offered by the Microelectronics Center will include systems and logic design, DA development, and multichip packaging as well as application and test capabilities.

These services will be available to other Honeywell divisions and to the external market through the corporation’s Digital Product Center in Colorado Springs, Colorado. The Digital Product Center was established two years ago to provide high-performance semicustom and radiation-hardened digital ICs to the merchant market.

Erratum

Figure 17 of Manuel d’Abreu’s tutorial, “Gate-Level Simulation,” appeared incorrectly in the December, 1985 issue of Design and Test. The corrected figure appears below.

Figure 17. Timing diagrams.