Manufacturing Testing

The Path to Successful Production

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Our industry, the world of design and test of computers, still runs at a fast pace. The demands of our customers and the intense competition among suppliers has resulted in a high-performance, high-tech race toward excellence. This effort, moreover, is no longer confined to national boundaries as expanded communications and transportation techniques bring the world and its variegated cultures and economics together in a curious mix.

The hard results of this dynamic process are seen in the birth and manufacture of a product, one that is offered to the marketplace as the conceived and nurtured child of a select breed in a harsh environment. As survival becomes a basic issue, a product must have been well planned to be brought to market with high quality at the right time, and at the competitive price. Successful ventures continue to prove that a product which is testable through its entire life cycle has a high survival rate. Thus, for this issue, we concentrate on one of these phases: a critical one called "manufacturing testing."

This phase is critical because the product is about to proliferate, to multiply, to be distributed. The product must be manufactured in a consistent, timely, controlled process whose parameters need constant monitoring and adjusting for a uniformly high-quality output. Manufacturing test in this context, then, is devoted to devising that design and control process which, through hardware and software techniques, assures a successful production run. Implied here are the many specifications and parts lists, the CAD links to CAM and CAT, the databases, and the testability guidelines and rules. In fact, the entire CAE process is itself exercised by the techniques of manufacturing test.

Software has received more and more attention as astute competitors recognize that the "programs" of verification, simulation, test, analysis and diagnosis are the key to systematizing not only the "good" process but the "bad" process as well. If sorted out intelligently, the latter is a measurable deviation from the former; and if the "good" process is the "expected" one, manufacturing test needs to be designed to feed back and correct the out-of-tolerance trends and failures.

The computer industry's basic unit of functionality has evolved from the vacuum tube to the VLSI chip. The well-known process of compressing circuit functionality from PWBs into smaller, faster semiconductor ICs, or "chips," has resulted in VLSI and VHSIC packages. But the PWB itself does not go away. Customers continue to demand more functionality and more reliability, at the same or lower unit cost. Thus, as circuits become denser and
they are put on chips, they must still be interconnected and that vehicle remains the PWB.

But both the PWB and the VLSI chip are in themselves marvels of the electronics age. They represent the industry’s answer to the interconnection of hundreds of electronic components in the smallest possible space.

Today’s PWB technology accommodates thousands of “lines,” or finely etched copper pads, as fine in width as 5 mils and only that far apart as well. This packing density is multiplied by vertically stacked multilayer layers sandwiched between power planes and ground planes. Vertical connections are made through vias in order to route lines up and over bothersome single-layer interconnections or to avoid parallel line capacitances which load and slow down high-speed signals.

Thus, a whole new industry has been spawned to automate the construction and test of the PWB. CAD workstations and software now assist the engineer in automatic placement, layout, routing, modeling, simulation, and test.

Keen international competition forces participants to keep abreast of frontier technologies such as multilayer boards, VLSI, micro-packaging and interconnections, volume assembly, and rapid test and diagnosis. Thus, as our semiconductor packages and PWBs are assembled into larger units and systems, the manufacturing test process becomes hierarchically structured and constructed.

To demonstrate the hierarchical structure, six papers have been selected for this special issue on manufacturing test:

In their article entitled “Inductive Fault Analysis of MOS Integrated Circuits,” authors John P. Shen, W. Maly and F. Joel Ferguson of Carnegie-Mellon University present the three major steps of their inductive fault analysis, or IFA, procedure. Their method generates physical defects using statistical data from the fabrication process, extracting the circuit level faults caused by these defects and classifying and ranking these faults based on their likelihood of occurrence. This fault list can be used to determine the actual effectiveness of test sets and guide the generation of better test patterns. An example is given, and the results lead to observations concerning non-classical faults as well.

In their article “PROD: A VLSI Fault Diagnosis System,” Peter Odyna and Andrzej J. Strojwas of the SRC-CMU Center for Computer Aided Design present a diagnostic system whose goal is to diagnose the source of faults that result in flawed chips. Faults occurring in the manufacturing process of VLSI chips lower the effective yield, thus increasing manufacturing costs. Fault diagnosis is achieved through analyzing the joint probability density function of measured IC parameters. The authors present their diagnostic algorithms and explore their implementation in a complete diagnostic system through several examples.

IBM’s Kofi E. Torku and Dave A. Kiesling then describe their experiences with noise during manufacturing test in a comprehensive article entitled “Noise Problems in Testing VLSI Hardware.” In this presentation, they provide some guidelines for both product and tester design to reduce simultaneous switching during test of bipolar VLSI chips and multiplex circuits. They point out that during the switching of high-current off-chip (or off-product) drivers in VLSI circuits, simultaneous switching can induce voltage spikes in the power supply. These voltage spikes can cause a register to lose its state, and without the appropriate measures either in the tester or during design of the product under test, the noise problem can lead to a zero yield at manufacturing test. They further point out that it is very difficult to conclusively distinguish a noise problem from a logical race condition or process defect.

Digital Equipment Corporation’s Tim Moore and Stephen Garner examine the problem of automatically probing printed wiring boards on a modern dynamic high speed functional tester. In their article, “Auto-probing on the L200 Functional Tester,” they explain the reason for developing an X-Y auto-probing process to eliminate the need to manually probe prototype modules and to diagnose production modules (populated printed wiring boards). Nodal verification is then established when the simulated expected results are matched. The goal of X-Y auto-probing is to increase the throughput of the functional tester by decreasing the average diagnostic time through automatically controlling the movement and positioning of the probe. This article describes a solution in both the hardware and software of a system which is being explored and implemented by several companies around the world.

David F. Farnholtz of the AT&T Technology Division, Allentown, Pennsylvania, provides a treatise on “Operational Life Testing of Electronic Components.” He describes a major effort to systematize and quantify the statistics of electronic components "infant mortality.” He develops a process called operational life testing to continuously monitor the early life failure and the failure mode analysis of OLT defects and implementation of the indicated process, testing, and design changes. This process has resulted in significant savings and enhanced component reliability for the author’s company.

In “Teradyne’s J967 VLSI Test System,” a special D&T product story, Wayne Ponik of Teradyne describes the newest member of the J900 series of VLSI test systems. He details the package, which is heralded to test the majority of VLSI devices with less than 200 leads and bus speeds up to 20 MHz. Ponik addresses the quality of test issue by examining the J967’s ability to provide flexible timing and formatting; fast, accurate parametric tests; and automatic calibration of the device under test.

For this special issue, we received a total of 14 submittals, from which the final six were chosen as representative of the spectrum across manufacturing testing. We are gratified by the response of the manufacturing test community, and I want to take this opportunity to thank all authors for their time and effort in contributing to such a comprehensive and challenging effort.

Likewise, the many reviewers (at least three, and sometimes five per paper) are here publicly recognized and especially commended for a job well done despite the anonymity required of the review process.

I hope our readers will enjoy this issue as much as we all enjoyed putting it together.

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Arabian is also the Manufacturing Test Editor for D&T. Since entering the electronics industry in 1950, he has written numerous papers and magazine articles, and received the best paper award at the 1982 Paris ATE conference. Arabian received his BA degree in engineering from Harvard and his MS from the Massachusetts Institute of Technology. He is a registered Professional Engineer and a member of IEEE, ISA, ASTE, AIAA, and British Society of Test Engineers.