GenRad reports $1.8 million second quarter loss

GenRad, Inc. reported a net loss of $1,824,000 for the second quarter ending June 29 as compared to its 1984 second quarter net income of $4,812,000, and a net loss of $1,694,000 for the six months ending June 29 as compared to its 1984 first-half income of $6,187,000. The loss of 11 cents per share was on second quarter sales of 58 million dollars; 1984's second quarter earnings of 30 cents per share was on sales of 63 million dollars. Anticipating fewer orders for automatic test equipment, Genrad cut its work force by 12 percent to reduce expenses in the first quarter. Further work force actions will be necessary as the year progresses, according to GenRad, unless business “materially improves.” In his report to stockholders, company president and CEO William R. Thurston stated that orders had dropped in the semiconductor test market, “particularly the computer market served by our printed circuit board test division. This slump has affected the entire automatic test equipment industry.”

New CS president is former D&T EIC

Roy L. Russo, founding editor-in-chief of IEEE Design & Test, has been elected president of the IEEE Computer Society for 1986. He will assume the post on January 1. Currently vice president for CS conferences and tutorials, Russo has served the Society in various leadership positions for more than 10 years. His contributions include initiating the Robotics, Personal Computing, Computer Languages, and Computers in Education technical committees, introducing the concept of a vice president for standards, and developing a uniform accounting system with the IEEE.

He also initiated the Computer Services Advisory Committee and has served on the Executive Committee, Governing Board, Design Automation Technical Committee, and various other committees and boards. After founding D&T, he served as the magazine's editor-in-chief from 1983 to 1985.

Russo is manager of the Design Automation Laboratory at the IBM T.J. Watson Research Center. An IEEE Fellow, he is a member of ACM, Eta Kappa Nu, and Sigma Xi. He holds a PhD degree in electrical engineering from Pennsylvania State University, and has won several awards for professional achievements.

Yamada elected to CS Governing Board

Akihiko Yamada, D&T International Editor/Far East has been elected to a two-year term on the IEEE Computer Society Governing Board, commencing January 1, 1986. Yamada, who was guest editor for D&T's October issue on design and test in Japan, arranged for the first translation of an original Japanese article for the magazine's November 1984 issue.

He has been an invited speaker at several international conferences in the design automation and test fields, and is active in IEEE and Japanese computer society projects. He is chief engineer at the EDP Systems Engineering Division of NEC Corporation, and is in charge of the planning and development of CAE/CAD systems.

Yamada holds a PhD degree from Osaka University, Osaka, Japan, and is a member of IEEE, the Institute of Electronics and Communication Engineers of Japan, and the Information Processing Society of Japan.

Hewlett-Packard plans Cericor acquisition

This September HP signed a letter of intent to purchase all the assets of Cericor Inc., subject to Cericor shareholder approval and governmental review. Leading up to this, Cericor and HP agreed in March to integrate Cericor's CDA 5000 software packages into HP's logic-design products for CAE application. HP first purchased an 11 percent equity position in Cericor in July.
$1.8 billion GaAs market predicted by 1990

Advances in material technology and crystal growth allowing fabrication of high-grade gallium arsenide, or GaAs, substrates will spur the market for such devices to $1.8 billion by 1990, according to a recent market study.

The first GaAs integrated logic circuits are now becoming commercially available, and monolithic analog ICs using GaAs are being introduced to replace previous discrete GaAs devices.

Gallium arsenide’s superior performance compared to silicon is expected to lead to a market surge from its current $60 million to $1.8 billion within five years, states market analyst Robert Castellano. During that time the military sector, currently representing 76 percent of the GaAs market, will drop to 30 percent; market growth will be led by the communications market, which will use 35 percent of all GaAs ICs in 1990.

The challenge GaAs poses to silicon should concern all semiconductor suppliers and system manufacturers, Castellano notes, since the compound will first boost the speed of supercomputers, then of mainframe, mini-, and ultimately microcomputer systems. Such processors are the engines of expert systems and other artificial intelligence applications, as well as CAD and CAE workstations.

Additional GaAs applications are anticipated in super-high-frequency devices used in satellite receiver systems, optical communication networks, and mobile telephone systems.

GaAs semiconductor manufacturers, meanwhile, face technological hurdles in chip testing and packaging, since high-speed testers and packages are not yet commercially available.


Integrated circuit testing and inspection

As IC complexity increases and customer requirements for high reliability become essential, the IC testing problem grows more acute. The four conflicting criteria are manufacturing throughput, final production yield, IC production cost, and in-service reliability. Innovative compromise solutions are required to reduce the nondetection and false alarm probabilities and to minimize the relative IC testing costs and testing time.

The Battelle research center of Geneva has therefore pursued the concept of integrated testing, designing a single test station and the corresponding procedures to carry out imaging, electrical, and environmental tests. Test station design may vary depending upon location in the manufacturing process. The main benefits of integrated testing are: the reduction of imaging and electrical inspection times; the reduction in nondetection and false alarm rates; the reduction or suppression of physical transfer time between test stations; the localization of defects to allow for better recycling or reject decisions; and the reduction of electrical test sequence length, for a given acceptable IC quality level, by using results of imaging and environmental tests.

The design of integrated testing relies on developments in artificial intelligence and pattern recognition; in custom sensors, instrumentation, and sensor fusion; and in statistical data analysis and the learning by expert systems of physical or software failure processes. These developments should be useful for digital and analog ICs and monolithic sensors used in high reliability data or electronic systems in automotive, aerospace, biomedical, marine, mining, and other applications. The same techniques may have an impact on other IC classes. The substrates to be considered are silicon, gallium arsenide, HgTe, and II-VI compounds.

For more information contact Dr. L. F. Pau, Battelle-Centres de recherche de Geneve, 7, route de Drize, CH 1227 Carouge/Geneva, Switzerland; 4122-439831; telex 23472-BATL-CH.

Mercer joins IEEE D&T editorial board

Melvin Ray Mercer has been named Design for Testability Editor for IEEE Design and Test of Computers. Mercer is an assistant professor of electrical and computer engineering at the University of Texas at Austin, and holds the Werner W. Dornberger Centennial Teaching Fellowship in Engineering there.

His research interests are in the areas of digital simulation, computer architecture, fault tolerant computing, and computer-aided design of VLSI devices. Before joining the University, Mercer was a member of the technical staff at AT&T Bell Laboratories, Murray Hill, New Jersey, where he worked on the CAD and testing of digital circuits. He also has industrial experience at Hewlett-Packard Laboratories in Palo Alto, California, and GTE Sylvania in Mountain View, California.

Mercer received his BS from Texas Tech University, Lubbock, Texas; his MS from Stanford University, Palo Alto, California; and his PhD from the University of Texas at Austin, all in electrical engineering. He is a member of Tau Beta Phi, Eta Kappa Nu, and chairman of the Central Texas chapter of the IEEE-CS. Mercer holds two patents in the area of design for testability, and received the best paper award at the 1982 International Test Conference.
Rigid disk industry unites to resolve test confusion

Delegates representing manufacturers of rigid disk media, heads, disk drives, and test equipment pledged to support the newly created test measurements and methods ad hoc group of the ANSI X3B7 disk standard committee. Group founder and chairman Frank B. Meijers urged cooperation beyond competitive boundaries to provide standardization in test methods and terminology.

According to Meijers, the industry has sought a single disk performance standard for years, while ignoring the fact that disks are presently used in different applications requiring different specifications. "At the same time," Meijers said, "there are no performance standards for disk drives and the terminology in most specifications is ill-defined."

Many test equipment problems, ranging from questionable design to improper use, add to the confusion—confusion leading to invalid data, poor correlation, uncertainty, and incorrect feedback for process control. "As a result," Meijers went on, "on an average day we may throw away thousands of perfectly good disks, rebuild thousands of quite acceptable HDAs and, worse yet, ship thousands of disk drives of marginal quality."

By drawing on industry experts, the committee hopes to proceed quickly, Meijers said. Active participation of test equipment manufacturers and commitments received from drive manufacturers and system integrators reflect the degree of interest in the group's activity, he added.

For further information or to make a technical contribution, contact Frank Meijers, president and CEO of Luctor Corp., Phoenix, AZ; (602) 864-1298.

Venture capital in high technology

Bohdan O. Szuprowicz
21st Century Research

American entrepreneurs depend upon, even require, venture capital. Venture capitalists favor high growth enterprises. This combination has assisted in producing new jobs, new tax revenues, and improving American productivity overall.

There is increasing awareness that the US will remain the undisputed leader in venture capital and high technology innovation despite a Japanese challenge. One reason is the escalating demand for venture capital as VLSI-based microelectronic products become more complex.

In the US is there enough venture capital available, since new start-ups may require $10 million or more in the initial rounds of financing; only in the US are the end-user markets big enough to justify such an investment.

High technology and venture capital are becoming new priorities in current geopolitics. Venture capitalists expect a minimum 30 percent rate of return, but few business proposals meet such an expectation. While venture capitalists find that half of the firms they start will be winners, and 15 percent will be losers even in the best of times, they are particularly active during recessions and slack economic periods if they foresee recovery and can maneuver to exploit unusual investment opportunities.

In order to maintain American leverage, there is continued pressure to reduce the capital gains tax rate to 17.2 percent, particularly in the face of rising competition from Japan, West Germany, Australia, Belgium, Italy, and the Netherlands, where there are no long-term capital gains taxes and where conditions for venture capital are being developed.

Teradyne celebrates silver anniversary

Founded in 1960, Teradyne, Inc. is celebrating its 25th year in the ATE industry. Today Teradyne has sales and service centers across the US, in Europe, and in the Far East. The firm recently released the J967, the latest of its J900 series of VLSI test systems. Our Product Story this issue deals with the J967.

Teradyne's semiconductor test division has also published a free 44-page booklet on the economics of VLSI testing, analyzing and showing how to calculate the total cost of a VLSI test system. The booklet is divided into five sections: the introduction, features of the Teradyne J941 VLSI test system, a sample manufacturer's model, model worksheets for device manufacturers, and a model worksheet for the device user.

For further information on the economics of VLSI testing, contact Teradyne, Inc., Inquiry Systems and Analysis, 660 Summer St., Building 114, Box 120, Boston MA 02210.

Motorola and NCR form ASIC alliance

Motorola and NCR have signed a five-year development and alternative source agreement encompassing both CMOS gate arrays and standard cell libraries to implement application-specific integrated circuits, or ASICS. In addition to the exchange of existing ASIC products, the agreement provides for joint product specifications, CAD software transfers, and cooperation to extend the resultant common libraries to future gate array and standard cell products.

Under the terms of the agreement NCR will transfer its three-micron CMOS II standard cell library containing analog cells, configurable memory and PLA, a 65CX02 core microprocessor, and an extensive digital logic library. Motorola will provide its two- and three-micron double-layer metal HCA6000 series CMOS macrocell array families. In addition, both companies are exchanging their advanced-technology two-micron standard cell libraries with double-layer metal.

A major feature of the agreement is the establishment of identical design automation interfaces, making the choice of supplier transparent to the design task. Motorola presently supports its HCA6000 macrocell array families on Daisy Systems and Mentor Graphics CAE workstations. Abilities include schematic capture, functional and performance simulation, and automatic place and route. NCR also provides total design capture and verification systems for the CMOS II standard cell library on both Daisy Systems and Mentor Graphics workstations. Both companies will exchange CAD tools and will participate in the evaluation and development of design automation.

Fundamental to this alliance is the establishment of working teams from many disciplines, responsible for making NCR and Motorola appear as mirror images.
Semiconductor industry invention and assessment

According to the Semiconductor Research Corporation, most foreign competitors in the semiconductor industry have some form of cooperative technology development program in place, while in the US each company must develop its technology base from scratch, particularly its manufacturing technology. As a result, Japanese semiconductor manufacturing technology is not only considered superior but is improving at an ever-increasing rate; their manufacturing technology base, established in part by the MITI VLSI program, provides results to most Japanese semiconductor manufacturers.

In contrast, the US manufacturer attempts individually to develop equivalent expertise because the US semiconductor industry since its inception has fostered and rewarded the entrepreneur at the expense of cooperative effort. An additional obstacle is the effective transfer of the generic technology from its development site to its place of commercial exploitation, SRC says. Unless a company has the resources required to compete with cooperative foreign efforts, it will fall further behind. And even when companies have the necessary resources, the duplication of effort and expenditure is wasteful.

Group leverage is key to resolving this dilemma, SRC goes on. If members of the US semiconductor industry pooled a fraction of their resources to develop a common technological base, increased leverage would enable each company to plow a greater share of resources into proprietary innovation.

Last summer, SRC conducted a technology assessment workshop to (1) evaluate the relative status of US and Japanese technology in the areas of bipolar ICs, memory, and arrays, and (2) to identify where improvement in US ability was needed and how such improvement could be obtained. The workshop was the first time that the SRC brought together scientists and engineers for an assessment of industry status.

Jeff Frey of Cornell University, currently a visiting professor at the University of Tokyo, made the following observations: Japanese science and technology funds are twice US NSF funds; MITI, the prestigious Japanese civil service, dictates the efficient use of Japanese resources; Japanese semiconductor investment was down significantly in 1984 as compared with 1983; Japan produces more EEs with BS degrees than we do, although theirs must be industry-trained three years before they are productive; Japan silicon thrusts include displays, low-resisitivity interconnects, SOI/3D ICs, and radiation-assisted processing, with work also being done in GaAs and HEMT technologies; the Japanese work well in groups, and use groups in parallel efforts effectively to solve problems within a company.

The bipolar session concluded that: bipolar ICs are here to stay; although the US has a competitive technology base in the lab, the Japanese are far more capable in manufacturing; Japan is driving hard in bipolar/CMOS while the US is weak; the US is dropping out of the high-speed bipolar memory race while Japan is working because of its supercomputer program; high-speed bipolar logic is being pushed hard in Japan and the Japanese are willing to increase the number of masks to obtain higher yield.

The memory session noted that in some respects the US is superior, although the Japanese are ahead in DRAM technology. The comparative percentage of papers presented at ISSCC from 1980 to 1985 has been reversed; in 1980 the US presented 62 percent and Japan 29 percent, but in 1985 Japan presented 66 percent and the US 34 percent.

The arrays session noted that gate arrays continue to be regarded as a viable design option because they offer a satisfactory compromise between the objective of rapid, low-cost IC production and the conflicting requirement of maximum circuit performance.

Tl purchases Carnegie Group equity

Late this summer TI purchased a 10 percent equity interest in Carnegie Group Inc., the research and development specialist in artificial intelligence, or AI, software. The Carnegie Group will use equipment credits acquired in the exchange to purchase TI computer hardware and software.

TI also signed a three-year general license agreement with the Group under which TI will fund research, experimentation, and development projects for AI software. Reciprocally, TI will receive technical training for senior AI personnel and a license to distribute the Group's technology and products internally.

The Carnegie Group focuses on applying AI to the manufacturing process, developing applications in automated engineering design including CAD, CAM, and CAE expert systems. Carnegie Group's concentration on expert system development, according to TI's executive vice president Grant Dove, enhances TI's manufacturing operations plus providing AI applications for use in their industrial, defense, and electronics divisions.

Hitachi increases US high-tech purchases

Last August a 16-member import promotion team from Hitachi of Tokyo visited 40 American companies in 13 states. The purpose of their visit was to purchase high technology US products including telecommunications equipment, computer hardware and software, manufacturing equipment, materials, R&D equipment, and semiconductors.

As a result of that visit, Hitachi announced purchases of approximately $40 million among 23 US companies, with 14 companies receiving orders ranging from $0.5 to $4 million. Those 14 companies were General DataComm Industries, Technology for Communications International Inc., Microsoft Corp., Moore Special Tool Co., Hewlett-Packard, GenRad Inc., National Electrostatics Corp., Amax Inc., US Reduction, Digital Equipment Corp., Cincinnati Milicron Marketing, Minster Machine Co., Tektronix Inc., and GE Calma.

These purchases were part of Hitachi's commitment to increase procurement of US goods; compared to the $260 million Hitachi spent here in fiscal 1984, the procurements are expected to total $350 million in fiscal 1985, and the intended $400 million in fiscal 1986. Another Hitachi team is expected to visit before year's end with approximately $10 million to spend in the semiconductor market.