Workshop on Simulation and Test Generation Environments

Sponsored by IEEE Computer Society and Test Technology Committee

September 17-18, 1985
San Francisco, California

You are invited to participate in the Workshop on Simulation and Test Generation Environments which will be held in San Francisco, California, September 17-18, 1985. The workshop is organized around the theme of surveying recent developments in software engineering environments for logic simulation and test program generation.

Circuit size and complexity are growing at a faster rate than can be addressed by improved simulation and automatic test generation algorithms or by faster computing resources. Thus the emphasis in addressing these problems is shifting from algorithms to environments which help the design and test engineers improve program generation productivity. The purpose of the workshop is to bring together researchers and practitioners from universities, industry and government to review the recent developments and identify new requirements on the software environments as applicable to logic simulation and test generation during design and test of digital circuits.

Topics of Interest

- Network compilation and simulation support programs, postprocessors
- Syntax and context-directed program editors, automatic revision tracking
- Graphic data synthesis, analysis and test program generation
- Component model library development and verification tools
- Model and test program debugging
- Tester environment simulation
- Test program set configuration management

All participants are expected to register through mail by August 30, 1985. There will be no at-the-door registration. Attendance will be limited to 60 persons based on the registration date. Call the Workshop Chairman for additional information about the program and possible late registration. Registration fee $140 for IEEE members, $175 for nonmembers.

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