More than ever before VLSI designers need a single CAD system that provides accurate, high-speed simulation of complex designs traversing all design levels - architectural, microcode, behavioral, RTL, gate, and switch. VERILOG takes you through all levels with a single homogeneous language.

The powerful and interactive symbolic debugger permits you to home in on design errors and even override them without terminating your mixed-level simulation. VERILOG's high speed compilation lets you build models in seconds and roll into simulation. It's a unique interactive tool for both design and simulation.

**Get on the Fast Track**

VERILOG handles even complex descriptions at speeds markedly faster than comparable systems. Simulating an 8085 microcomputer on a small 68010-based workstation, VERILOG barrels along at seven instructions per second - after building the model in six seconds flat. Gate and switch level simulation speeds rival those of gate-level only simulators.

**With Interactive Control**

Because VERILOG is interactive, testing and revising a design is efficient and flexible. A sophisticated symbolic debug with highly selective source trace tells you what is being simulated along with results. You can pinpoint problem areas quickly, update the design, and return to simulation in record time - a truly interactive process. Convenient batch-mode processing provides maximum flexibility.

**Ride the Right Track**

A single homogeneous language at all levels for design description, waveform description, expected responses, symbolic debug, and interaction - all in VERILOG. You can link most software programs with your hardware description in VERILOG and simulate your software with your hardware design. A large SSI/MSI model library facilitates PCB design. VERILOG runs on a host of machines - Apollo, Sun, DEC/VAX, UNIX machines, and soon, IBM.

Fast, flexible, and functional, VERILOG lets you coast to successful logic design.