June 1986

Design Automation Conference (ACM), June 22-25, Las Vegas, Nevada. Contact J. D. Nash, Raytheon Co., Bedford, MA 01730; (617) 274-7100, ext. 4758.

October 1986

ICCD 86, International Conference on Computer Design, October 5-10, Atlantic City, New Jersey. Contact ICCD 86, PO Box 639, Silver Spring, MD 20901; (301) 589-8142; TWX 7108250437 IEEECOMPSO.

Design Automation Workshop, October 8-10, Lansing, Michigan. Contact Design Automation Workshop, PO Box 639, Silver Spring, MD 20901; (301) 589-8142; TWX 7108250437 IEEECOMPSO.


Cadence West 86, Conference on Computer-Aided Engineering and Computer-Aided Design: January 7-9, 1986, Anaheim, California. Papers on recent and novel developments in all areas of computer-aided engineering and design are sought. Submit abstracts (200 to 500 words) by July 1, 1985, to Art DeSena, Morgan Grampian Expositions Group, 1050 Commonwealth Ave., Boston, MA 02215; (617) 232-5470.

First International Workshop on VLSI Design: December 26-28, 1985, Madras, India. Send abstracts (400 words maximum) by July 1, 1985 (and inquiries about participation), to H. N. Mahabala, Dept. of Computer Science and Engineering, Indian Institute of Technology, Madras 600036, India, or Vishwani Agrawal, AT&T Bell Laboratories, Murray Hill, NJ 07974; (201) 582-4349.

Compcon Spring 86: March 3-6, 1986, San Francisco, California. Participation in the form of a technical presentation or the organization of a session on state-of-the-art topics for computer professionals is sought. Persons wishing to make presentations are asked to send four copies of a 500-word abstract by July 15, 1985, to Alan G. Bell, Xerox Palo Alto Research Center, 3333 Coyote Hill Rd., Palo Alto, CA 94304; (415) 494-4326. Persons wishing to organize sessions are asked to contact Bell by the same date and to include with their ideas a list of possible speakers.

1986 International Conference on Robotics and Automation, April 14-17, 1986, San Francisco California. Papers are solicited in all areas of robotics and automation, with special emphasis on aspects such as flexible manufacturing, material handling, scheduling and control, system design and control, modeling and simulation, and economic evaluation. Specific topics include CAD/CAM, and planning and scheduling in robotic automated systems. Submit four copies of a full-length paper (15 to 20 double-spaced pages) by October 1, 1985 to Rajan Suri, Dept. of Industrial Engineering, University of Wisconsin-Madison, 1513 University Ave., Madison, WI 53706. For more information, contact Robotics and Automation, (301) 434-1990.

D&T Standards

Editor: Harold Carter, Air Force Inst. of Technology, Wright-Patterson AFB, AFIT/Eng, Dayton, OH 45433.

It is a pleasure to serve you as standards editor. It is my intention to bring you the most up-to-date news and articles concerning standards efforts within the computer design and test fields, and I eagerly solicit your contributions. Please forward meeting minutes, summaries of standards actions, brief articles (1000 words or less) or other standards-related information to me, preferably in publishable form.

H. W. C.

Standards to keep IC fabrication costs down

The Defense Advanced Research Projects Agency (DARPA) is preparing to offer a low-cost, rapid-prototyping fabrication service via its MOS Implementation Service (MOSIS) by January 1986.

Chip designs will be required to use a standard pad-layout frame, a single die size, a standard dip package, and a process design-rule sets. Based on standard MOSIS, 3-micron CMOS and NMOS single foundry-based processes, the service will be oriented towards prototype circuits. At an anticipated cost of $250 for CMOS and $200 for NMOS, three to six parametrically tested chips are returned to the designer within eight weeks after the design has been submitted in CIF format.

Using one of several design frames (see "VLSI system design by the numbers," IEEE Spectrum, February 1985), the designer will lay out his circuit and submit it to MOSIS for fabrication. MOSIS will add the design-frame layout to the designer's layout and then submit it for mask generation and subsequent fabrication.

In part, the low cost per chip will be a result of the large number of designs being fabricated per wafer. After processing, parametric testing and packaging, the chips will be returned to the customer for further functional testing and evaluation. The use of standard frames, pad-layouts, processes, and chip and package sizes is also expected to help keep costs down. This set of complete yet flexible standards—all specified by the MOSIS service provided by USC's Information Science Institute under contract to DARPA—will provide for maximum use of processing, testing, and packaging automation.

New version of the VHDL hardware description language

Version 7.0 of the DoD VHSCIC Hardware Description Language (VHDL) has been released, reflecting a number of changes suggested by an industry/academic review panel. The new version provides a better representation of configuration information, improves the decomposition of large behaviors, permits mixed behavioral and architectural descriptions, clarifies the distinction between inertial and transport delays, and includes the specification of the initial state of a description.

It is anticipated that Version 7.0 will be the baseline description of VHDL during the current implementation phase by Intermetrics, Texas Instruments and IBH.