can be used only for regular structures arranged in a well-partitioned data flow. It does not address the problem of testing the irregular types of logic found in the control sections of computers. Also, it does not offer a push-button solution to test problems, as do conventional automatic test pattern generation, fan-out cutting, or pseudo-exhaustive test. Instead it requires extensive investigations by a skilled engineer, using the "rules of thumb" described earlier. Design automation "purists" might also argue that anything done manually is unreliable and so should not be used.

On a more detailed level it is obvious that this methodology places strict constraints on the placement of registers within the data flow, possibly imposing overhead on the chip size. However, this problem is not nearly as serious as it might appear. Investigations have shown that registers can be shared and that test pattern sequences can be routed through the data flow. This is currently the subject of ongoing research. □

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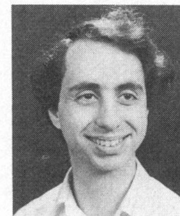

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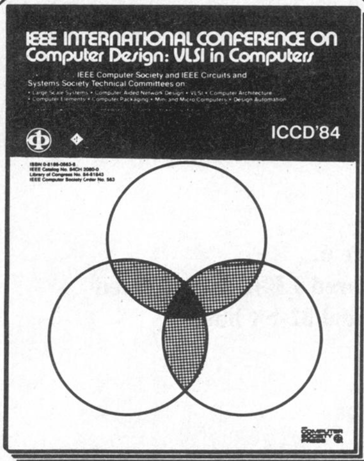

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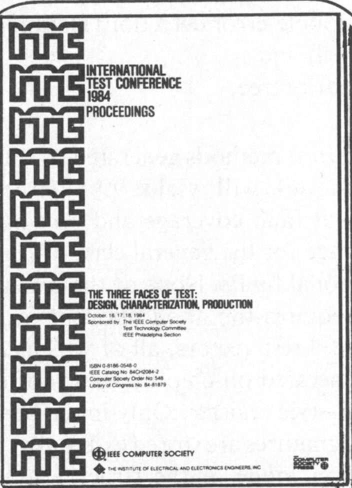

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