Technical program addresses

The 1985 Test & Measurement World Expo, May 14-16 at the San Jose, California, Convention Center, will feature technical sessions and an exhibition.

During the three days, 24 technical sessions with over 100 papers will focus on test, measurement, and inspection, particularly as these topics relate to the factory of the future. Sessions of particular interest include “Memory Testing Challenges in the 80’s,” “Testing of Surface-Mounted Devices,” “Software Issues in Test and Measurement,” and “Future Factory Test and Measurement Concepts.”

The expo includes a four-day course entitled “Automatic Testing Technology: Hardware & Software Systems.” Exhibitors will display a wide range of equipment, including CAD/CAE/CAT and ATE systems.

Complete details of the technical program and course are available from Meg Bowen, Conference Director, Test & Measurement World Expo, 215 Brighton Ave., Boston, MA 02134; (617) 254-1445.

IBM's VLSI academic initiative

IBM's Federal System Division in Manassas, Virginia, has established a VLSI program with the University of Illinois, Pennsylvania State University, and Purdue University. This program allows universities to use IBM’s Master Image chip design system and methodology. Students design 4.2 mm x 4.2 mm, 2-micron NMOS Master Image chips. Each contains 560 cell locations. This Master Image provides a sufficient area to implement nontrivial designs, but also limits the design complexity to a manageable semester project.

Students are provided with a macrocell library of predesigned functional blocks ranging from inverters to highly automated placement and wiring facilities, allowing designers to concentrate on logic design and functional verification.

The unique feature of this arrangement is the design methodology and test requirements levied on the designer.

Only a limited number of designs which pass rigorous logical, physical, and testability rule checks may subsequently be selected by the professors to be fabricated by IBM. Fabricated chips returned to the student designers are accompanied by the results of stuck fault verification testing.

Complete closure of the design process is obtained by the student designer functionally testing the chip and verifying that it performs its predicted logic function. The chips are packaged in 48-pin dual in-line packages with 43 I/O connections.

The hardware portion of the design facility is centered around an IBM 4341 computer or its equivalent. Schematics and physical layouts can be viewed on a Tektronix 618/614 storage display terminal. More information can be obtained from N. C. Panella, IBM Federal Systems Division, 9500 Godwin Dr., Manassas, VA 22110.

Intel's CMOS EPROM gets first IC mask copyright

In early January, Intel's 27C256 CMOS EPROM chip became the first chip to be registered under the new Semiconductor Chip Protection Act of 1984. Motorola, Inc., and Harris Corp. reportedly also registered a MC68020 32-bit microprocessor and a 64K PROM, respectively.

To secure protection, owners of mask works must apply for registration of their claims with the copyright office. Owners must register their works within two years after the date on which the mask work is commercially exploited, or the opportunity to gain protection under the act will be lost.

Protection for a mask work begins on the date the work is registered with the copyright office, or on the date the mask work is first commercially exploited anywhere in the world. Protection lasts for 10 years.

To apply for registration of a mask work, a completed Form MW and a nonrefundable $20 filing fee must be sent with the appropriate identifying material to Register of Copyrights, Department MW, Library of Congress, Washington, DC 20540. Form MW can be obtained free of charge by sending a request to Information Section, LM-401, Copyright Office, Library of Congress, Washington, DC 20540, or by calling the forms hotline at (202) 287-9100.

Sentry discontinues showing at Semicon West

Sentry Test Systems (previously Fairchild Component Test Systems) says that it will no longer show its products at Semicon West. Instead, Sentry will demonstrate its test systems at its own West Coast facilities. The company feels that in-house demonstrations are more effective, particularly for large, high-technology, high-pin-count systems such as the Sentry 50 VLSI and the Series 80 analog/digital test systems.

During Semicon West, Sentry will conduct an open house at its San Jose, California, facility. A broad range of memory, digital, and analog products will be on display. Visitors will also have the opportunity to preview new products and to inspect the company's engineering, research, and production facilities.

Sentry notes that it will continue to participate in Semicon technical programs and that it will exhibit products at the International Test Conference November 19-21 in Philadelphia.

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