GenRad, LTX, Sentry, Teradyne seek larger Japan market

US test system manufacturers are increasing their market share in Japan by introducing new products, starting local manufacture, and improving product support. In a joint venture with Tokyo Electron, GenRad has started manufacturing VLSI test systems in Japan. LTX, Sentry, and Teradyne have announced that they will start assembling test systems in Japan this year.

US manufacturers, expecting a 40-50 percent increase in the Japanese market for test systems in 1985, are attempting to challenge the overwhelming Japanese market share held by Ando Denki and Takena Riken. Previously, American manufacturers have concentrated on the linear test market, an area not strongly addressed by Japanese companies.

Two factors are said to be behind US companies’ renewed endeavors in Japan. Japanese ATE companies are beginning to introduce linear test products. The Japanese market for memory and logic testers represents a huge potential market that American ATE companies cannot afford to ignore.

LTX has contracted for factory space in Tamachi, Tokyo, and will begin production of its linear IC test systems early this year. In addition to assembly in Japan, LTX plans to start software development. As well as trying to increase its current installed base of about 100 linear test systems, LTX plans to sell the new CMOS digital test system soon to be introduced by its subsidiary, Trillium.

GenRad recently announced the GR-14 VLSI test system, a Japanese-designed and Japanese-manufactured version of the American GR-16 VLSI test system. Selling for about half the price of most VLSI test systems, GenRad hopes that the new system will provide a foothold in the Japanese market for digital test systems. The first shipment of the GR-14 is planned for March.

Sentry, with an installed base of some 300 VLSI test systems in Japan, expects to have US volume production of the new Sentry 50 system by the middle of the year. The company has already announced a low-cost version of the system. In addition, some Sentry systems will be manufactured in Japan.

Teradyne, a long-time successful seller of linear test systems in Japan, is putting increased efforts into selling VLSI and memory test systems. The company has already started assembly of MSI/SSI test systems in Tokyo. One mark of the company’s stepped-up efforts in Japan is the publication of Japanese-language versions of the J941 VLSI test system and J386A-8 eight-in-parallel memory test system brochures.

Teradyne’s recently formed Japan Engineering Center has a mission to stay close to Japanese customers while maintaining strong ties to US technology. The group’s 20 employees have already developed products related to laser repair of DRAMs, hardware for testing image sensors, and a low-cost digital module for analog LSI testing. As a result of local design, local manufacture, and improved support, Teradyne is looking for a 30 percent sales increase in 1985.

Robotics, CAD/CAM marketplace defined

A new book, Robotics, CAD/CAM Market Place 1985, published by Bowker in January, claims to be a comprehensive guide to “a promising new world.” The book is said to include over 6000 listings of reference materials, products, organizations, databases, educational institutes, research laboratories, publishers, manufacturers, and scientific and technical specialists. Coverage ranges from the purely technical aspects of robotics and CAD/CAM to the social, economic, and human factors.

An introduction, written by Ken Susnjara, provides an overview of the robotics and CAD/CAM fields as they are today. Susnjara is president of Thermwood Corp., a company active in the field of robotics.

Information is available from R.R. Bowker Company, PO Box 1807, Ann Arbor, MI 48106; (800) 521-8110.
Computer-aided engineering market study published

In the February issue of Design & Test, we briefly referenced Prime Data's CAE Market Study. Since then, we have had an opportunity to study the complete volume and can provide more information.

The thick, loose-leaf volume is divided into five major sections: industry, market, competition, companies, and appendices.

The industry section begins with an overview of what Prime Data calls the computer-integrated industry, dividing it into computer-aided engineering, computer-aided design, and computer-aided test segments. Although the study focuses on computer-aided engineering, overlap between the three segments results in some discussion of CAD and CAT. The remaining pages of the section provide an overview of CAE history, applications, and markets.

The markets section provides detailed information about CAE markets for 1981 through 1983, estimates for 1984, and forecasts for 1985 through 1988. Market information is broken down by application, CAE vendor, product (hardware and software), geography, and end user.

In the competition section, there is a page for each major CAE vendor in which sales dollars for each major equipment category are listed for 1981 through 1983.

The companies section provides five-year financial histories, product-area breakdowns, and analyses of products for nine major suppliers of CAE hardware and software.

The first three appendices contain detailed tables of CAE vendor, geographic, and end-user market shares. The fourth appendix lists the worldwide economic factors that is part of Prime Data's database.

The study is part of Prime Data's new Computer-Integrated Service, which also includes regular newsletters, an inquiry service, and an annual conference. For information, contact Prime Data, 4030 Moorpark Ave., Suite 110, San Jose, CA 95117; (408) 249-7111.

Sami named D&T European editor

Mariagiovanni Sami has been appointed IEEE Design & Test's second European editor, Editor-in-Chief Roy L. Russo announced. Sami, who is based in Milan, Italy, joins H. Gordon Adshead, who is based in Manchester, England.

D&T's third international editor is Akiko Yamada of Tokyo, Japan.

Sami has been engaged in research and teaching at the Department of Electronics at the Polytechnic University of Milan, where she has been a full professor of computers since 1981.

Her research activities are in the area of computer engineering; for several years she has been active in fault-tolerant architectures, with particular concentration in distributed systems and VLSI architectures. Sami has published more than 50 scientific papers and books, mostly at the international level.

Her current research activities are partially funded by the European Economic Community under the Program for Support to Research and Development in the Area of Microelectronics. Sami is responsible for the activities of the Polytechnic University in Project CAD for VLSI in Telecommunications, a project that involves about 25 European research centers. She is also the leader of Project CVT's Subtask 3.1, Design Techniques for Fault-Tolerant VLSI.

Sami is one of the founders of EURONMICRO—the European Association for Microprocessing in Microprogramming—and she is editor-in-chief of Microprocessing and Microprogramming, the Euromicro journal. She served as organizing chairperson of the Euromicro Symposium in 1976 and program chairperson of the Euromicro Symposium in 1980.

Sami received her Dr. Ing. degree from the Polytechnic University of Milan in 1966. She is a member of both the IEEE and the IEEE Computer Society. She was chairperson in 1983 of the Steering Committee for FTCS 13.

SIGDA funds the compilation of DA bibliography

The ACM's Special Interest Group on Design Automation will compile a bibliography of design automation literature. "SIGDA's objective in establishing a grant for this project is to provide added service to its membership in industry, for whom library services are often less available than for those in academia."

The proposal deadline was February 15, and awards will be made by May 15. Work must be completed by June 1, 1986. A paper on the work will be required for presentation at the 1986 Design Automation Conference in Las Vegas, Nevada.

The terms of the award are flexible: one or multiple grants may be awarded, up to a total of $25,000. Selection of awards and administration of the grants will be conducted by a committee of SIGDA officers and directors. More information can be obtained from Charles A. Shaw, Chairman, SIGDA, GE-Intersil, 10710 N. Tantau Ave., Cupertino, CA 95014; (408) 996-5444.
AT&T grants $2.5 million to engineering schools

The AT&T Foundation has announced grants totalling $2.5 million to 34 major colleges and universities in support of science and engineering programs. "These special-purpose grants in science and engineering are an integral part of our overall effort to support higher education," said Kumar Patel, chairman of the foundation's Technical Grants Review Committee. The grants will go to areas that AT&T considers increasingly important to the future of information technology and the nation's economy. Among the schools receiving grants are Stanford University, the Massachusetts Institute of Technology, Cornell University, the University of California, Berkeley, and the University of Illinois, Urbana. The primary fields funded were electrical engineering, computer science, materials science, and physics.

The AT&T Foundation, which awarded its first grants this year, is the principal philanthropic group for AT&T and its subsidiaries. While emphasizing the support of higher education, the foundation also awards grants to leading institutions in the areas of social action, health, and the arts. Through its education program, the foundation also matches the gifts of all AT&T employees to colleges and universities, and provides financial aid for their capital and developmental needs.

VLSI Research surveys semiconductor industry

VLSI Research, a firm specializing in providing information and consulting services to the VLSI industry and its suppliers, has released its overview of the semiconductor industry. According to VLSI Research, the semiconductor industry consists of 407 competitors, with the majority in the US and Japan. Semiconductor manufacturers based in the US accounted for 52.5 percent of the market in 1983. Japanese manufacturers were responsible for 35.5 percent. Europe was another important area of production, as were several new emerging production areas, including Taiwan, Korea, India, and China.

In 1983, worldwide sales of semiconductor manufacturers grew by 24 percent. Total worldwide semiconductor shipments for 1984 were almost $34 billion, representing a 38.5 percent increase over 1983. The top 15 semiconductor manufacturers accounted for 61 percent of the total world supply of semiconductors. Texas Instruments continued to be the largest supplier. The second position was shared by Motorola and NEC.

Capital expenditures by semiconductor manufacturers in 1984 amounted to $9.3 billion, an 89.9 percent increase over 1983, according to VLSI Research. Of the three main geographic areas, the US has consistently spent the largest amount on capital investment, measured both in terms of dollars and percentage of sales.

The rapid growth in the overall electronics industry is responsible for the 38.8 percent growth rate of the semiconductor industry. Except for the solar power industry, electronic equipment is the sole source of demand for semiconductors.

While electronics have become an integral part of life, it accounts for just over two percent of the GNP, leaving plenty of room for growth.

For additional information, contact G. Dan Hutcheson, VLSI Research, Inc., 1754 Technology Dr., Suite 226, San Jose, CA 95110; (408) 289-9983.

| VLSI Research’s estimate of current and future worldwide semiconductor shipments in millions of units |
|-----------------|----------------|----------------|----------------|
| Type            | 1983          | 1984          | 1985          | Compound annual growth rate |
| Logic           | 8971.8        | 14182.7       | 24716.1       | 22.5%                     |
| Memory          | 1523.6        | 2371.4        | 5634.3        | 29.9%                     |
| DSP             | 1019.9        | 2060.7        | 8396.9        | 52.1%                     |
| Linear          | 4029.7        | 6100.8        | 11329.2       | 23.0%                     |
| Discrete        | 59768.1       | 62542.0       | 73637.7       | 4.3%                      |
| Photoelectric   | 5430.0        | 5872.1        | 7564.1        | 6.9%                      |
| Total           | 80743.1       | 93129.7       | 131178.3      | 10.2%                     |

3M, Bellcore become MCC shareholders

3M and Bell Communications Research have become the 20th and 21st shareholders in the Microelectronics and Computer Technology Corporation, a joint venture in Austin, Texas, of US corporations conducting advanced microelectronics and computer technology research.

Announcing his company's involvement, Lewis Lehr, 3M chairman and CEO, said, "By joining MCC we feel that we can take advantage of the effort being made toward developing the next generation of electronics."

According to Bobby Ray Inman, chairman, president, and CEO of MCC, "3M's diversity brings an important perspective to our organization, emphasizing the potential application of MCC innovations to a wide range of technologies." Inman said, "Bellcore's commitment to excellence and technological advancement represents the kind of philosophy that will be a key to MCC's success."

Bellcore, formed upon the divestiture of the Bell System, is a centralized technical support for seven regional phone companies. 3M will initially be involved in MCC's semiconductor packaging program, while Bellcore will concentrate on software technology and computer architecture.

The other MCC shareholders are Advanced Micro Devices, Allied, BMC Industries, Boeing, Control Data, Digital Equipment, Eastman Kodak, Gould, Harris, Honeywell, Lockheed, Martin Marietta, Mostek, Motorola, National Semiconductor, NCR, RCA, Rockwell, and Sperry.

AMD buys 100th Teradyne J941 VLSI test system

Just two years after the first J941 VLSI test system was shipped, Teradyne has announced receiving an order for the 100th system. That system was shipped to AMD.

Commenting in a recent issue of its monthly newsletter, VLSI Research noted that Teradyne was an early participant in the VLSI test system market. Since the J941 was introduced, however, the company has emerged as the leading supplier of VLSI test equipment and is shipping J941s at a rate greater than one a week.

David Braje, test operations manager of AMD's newest MOS wafer fabrication operation in Austin, Texas, received the 100th J941 and will use the system to test MOS microprocessors and microprocessors, including the 80286.
Gould AMI opens center for IC design

Gould AMI Semiconductors has opened a 5000-square-foot center that provides equipment manufacturers with all the hardware, software, and personnel support necessary to design application-specific ICs.

The design center, at the company's Cupertino, California, facility, provides complete services for businesses that want gate array and standard cell ICs, but do not have in-house design resources. Gould will rent space and computer time at the center and will also act as a foundry to fabricate the circuits designed there.

The center has 10 separate offices for visiting companies, each large enough for two or three people. Each office is equipped with a color graphics terminal, a symbolic layout terminal, or a commercial workstation. The offices can be locked and are soundproofed to ensure privacy. Group facilities include a conference room, a software demonstration area, and two training rooms where Gould personnel regularly conduct gate array and standard cell design classes, as well as classes in the use of Gould software and commercial workstations. Training and applications engineers are available for support.

Arrangements to use the design center can be made by contacting the Gould AMI headquarters at 3800 Homestead Rd., Santa Clara, CA 95051; (408) 246-0330, or through any sales office.

BNR uses voltage contrast to test IC designs

Bell-Northern Research scientists have started using a new voltage contrast process to look inside operating ICs and to help ensure the reliability of custom chips. The process enables designers to analyze and verify circuit designs at a very early development stage by viewing slow-motion pictures of electrical signals as they pass through complex ICs.

Voltage contrast involves placing an operating IC inside a modified scanning electron microscope. An electron beam is used as a strobe light to view the operation of the circuit in slow motion. Voltages in the circuit appear on the microscope's monitor as contrasting shades of black and white, enabling designers to detect and analyze design or fabrication flaws.

Frank Shepherd, manager of materials analysis at BNR’s advanced technology laboratory in Ottawa, said the voltage contrast technique is an improvement over conventional mechanical probes because it allows engineers to examine large areas of the circuit operating simultaneously. “Moreover,” he said, “circuit lines are becoming smaller. Mechanical probes are becoming very difficult to use because of their relatively large size, and voltage contrast may soon be the only efficient way to test internal areas of highly complex prototype integrated circuits.”

Once perfected, custom ICs designed at BNR are manufactured by Northern Telecom Electronics for the corporation’s telecommunication and information-management systems.
Josef Sukonick is the newly appointed senior development technologist at Valid Logic Systems.

Valid appoints Sukonick development technologist

Valid Logic Systems, of San Jose, California, has appointed Josef Sukonick as a senior development technologist. Sukonick will report to Tom McWilliams, vice president and a founder, and will initiate new developments for CAD/CAE products.

Before joining Valid Logic Systems, Sukonick served as vice president and chief scientist at Cadtrak, an architectural CAD/CAM workstation manufacturer. In 1975 Sukonick founded NuGraphics to develop CAD technology for the architecture, engineering, and construction industry. NuGraphics was acquired by Cadtrak in 1981. From 1970 to 1975, he directed technology and product development at Calma/GE.

Sukonick obtained his PhD in mathematics from Massachusetts Institute of Technology and his BS in physics at the University of Pennsylvania. He has held Woodrow Wilson and National Science Foundation fellowships and won the National Putnam Mathematics prize in 1964. He holds over 25 US and foreign patents.

AT&T to manufacture megabit CMOS DRAM chip

AT&T Bell Laboratories in Allentown, Pennsylvania, has developed a 1M x 1 CMOS dynamic random access memory chip with 1.3-μm design rules. The design team has stressed manufacturability, chip yield, and reliability with extensive computer simulations.

The one-megabit DRAM uses a single 5-volt power supply with on-chip substrate bias generation and has a typical access time of 80 nanoseconds. Its die size is 4.8mm x 14.5mm and is packaged in an 18-pin, 300-mil plastic DIP. A mask option would allow the DIP pinout to meet the proposed JEDEC standard or an evolutionary pattern compatible with the standard 256K DRAM 16-pin package pinout. As an option for the metal mask, the DRAM can support either a conventional page mode or a novel fast column mode which simplifies the board-level timing at data rates up to 20 MHz. The new megabit DRAM holds four times the amount of memory in the same area of the 256K DRAM fabricated by AT&T in 1982 yet needs only half the operating power and two-thirds of the access time.

Thomas R. ThompSEN, president of the AT&T Technology Systems Group, said that the race toward a production-line megabit chip was the Kentucky Derby of the semiconductor industry. "We'll see the unique influence of the megabit chip as designers learn how to combine it with other leading-edge technologies, such as the 32-bit microprocessor, and innovative software architectures," ThompSEN said. "These two next generation chips could be the foundation of powerful and easily portable computers. In the not too distant future, they could help put a supermini in business, industrial, or other special environments where space is a premium, or, for that matter, in your lap."

AT&T expects to be ready for manufacture in quantity by the end of this year and in full production in 1986. The technical details of the chip design were presented in February at ISSCC in New York City.

Zycad publishes design evaluation newsletter

Zycad, the manufacturer of the Fault Evaluator fault simulation system, publishes Zylene, a four-page newsletter that contains news about the company and its products. For information, contact Zycad, 3499 Lexington Ave, North, St. Paul, MN 55112; (612) 631-3175.

Separately, Zycad announced that it has delivered the first two Fault Evaluator systems to beta sites at Digital Equipment Corporation and Data General.

Accutest and Megatest make acquisitions

Accutest, a privately held manufacturer of memory, logic, VLSI, and parametric test equipment has purchased Basic Test Systems, a maker of linear device test systems. The undisclosed terms of the acquisition were for stock and cash.

Basic Test Systems, which currently employs about 35 people, began shipment last October of its first product, the BTS01.

Megatest, meanwhile, announced that it has acquired Parallel Systems of Santa Clara, a manufacturer of device handlers.

MOSAID sells DRAM design to US, Japanese companies

MOSAID has sold the design for a 256K dynamic random-access memory to a US and a Japanese semiconductor company. MOSAID President Dick Foss claims that the DRAM design can be fabricated with simple extensions of the process technology currently used to build 64K DRAMs. This claim is based on not using Polyicide processes which the company judges to have a high risk.

Founded in 1975, MOSAID is known for its MOS memory designs as well as for a series of design analysis reports which examine commercial ICs.
Tektronix acquires CAE

Tektronix has announced it will acquire CAE Systems, subject, at press time, to a number of conditions including the negotiation of a formal agreement and formal approval by the two companies.

Privately held CAE has about 140 employees and is based in Sunnyvale, California. The company offers design-capture and design-verification capability with its CAE 2000 software that runs on Apollo and Sun workstations, and on Digital Equipment’s Vax super-minicomputers.

Tektronix, a slow starter in the CAE business, clearly sees its acquisition of CAE as a major step in its ambition to be among the leaders. Outbidding rival buyers, rumored to include Hewlett-Packard, Gould, Lockheed, and Perkin-Elmer, Tektronix is said to have paid $75 million for CAE’s know-how and product line.

Tektronix sees the combination of its test and measurement capabilities with its own and CAE’s software expertise as the basis for a powerful solution to design problems for electronics systems designers. The company says, “The market now demands a full-fledged database that can serve as the foundation for integration of other tools. CAE Systems provides a way to offer that critical link to our (Tektronix’s) customers. We are fully committed to being a leader in this exciting and high-growth CAE market.”

The company believes that the acquisition of CAE gives it an immediate market presence.

Tektronix plans to port CAE software to the 6000 family of workstations. The integration of CAE software with layout software products from Tektronix’s VR Information Systems subsidiary and applications software from the company’s Design Systems Division is said to provide a comprehensive line of integrated CAE tools.

Gateway Design Automation specializes in CAD tools

Gateway Design Automation Corp., located in Littleton, Massachusetts, was incorporated in August 1982 with Prabh Goel as its president. Goel has nine years of technical and managemen experience at IBM and Wang. Co-founders are Barry Rosales, formerly of IBM; Philip Moorby, formerly of Cirrus Computers and the principal architect of HILO-2 and a key contributor to HTEST; and Chi-Lai Huang, an expert in the automation of logic synthesis. Both Goel and Rosales received IBM Outstanding Innovation Awards while at IBM.

Gateway offers a number of products and services in CAD software for design verification and testing of very large digital circuits contained on LSI/VLSI chips or on complex cards and boards. Its Verilog integrates the capabilities of behavioral-level languages such as N2, register-transfer-level languages such as ISP, gate-level languages such as Tegas-V, and switch-level languages such as BIMOS. Verilog provides symbolic debugging facilities for the designer to find design errors at all levels of digital design description.

Other CAD tools include AIDSSIM, for interactive logic and concurrent fault simulation at the gate/switch level; AIDSTG, for generation of integrated tests based on the scan design discipline; and PCLIB, a gate-level model library for most of SSI/MSI integrated circuits.

GDA is privately financed. By July 1984, its second year sales rose to $60,000 from the first year sales of $60,000. Additional information can be obtained from Gateway Design Automation Corp., PO Box 1545, 235 Great Rd., Littleton, MA 01460; (617) 486-9701.

April 1985

IMP selects Robinson director of customer tooling

International Microelectronics Products appointed Marc Robinson as the director of its customer tooling business. Robinson will report to Zvi Grinfs, senior vice president of business groups and will be responsible for all aspects of the silicon foundry business at IMP.

Most recently Robinson was with Advanced Micro Devices as operations manager for its MOS ATD fabrication area and manager of planning and administration for corporate technology. Before coming to AMD, he held management and technical positions in American Microsystems, Inc., Monolithic Memories, National Semiconductor, and AT&T Technologies.

Robinson holds a BS in physics from the Cooper Union in New York City and an MS in physics from Franklin and Marshall College in Lancaster, Pennsylvania. IMP, headquartered in San Jose, California, designs and manufactures standard cell-based CMOS VLSI circuits and offers 3- and 5-micron CMOS and NMOS processes.
Technical program addresses

The 1985 Test & Measurement World Expo, May 14-16 at the San Jose, California, Convention Center, will feature technical sessions and an exhibition.

During the three days, 24 technical sessions with over 100 papers will focus on test, measurement, and inspection, particularly as these topics relate to the factory of the future. Sessions of particular interest include "Memory Testing Challenges in the 80's," "Testing of Surface-Mounted Devices," "Software Issues in Test and Measurement," and "Future Factory Test and Measurement Concepts."

The expo includes a four-day course entitled "Automatic Testing Technology: Hardware & Software Systems." Exhibitors will display a wide range of equipment, including CAD/CAE/CAT and ATE systems.

Complete details of the technical program and course are available from Meg Bowen, Conference Director, Test & Measurement World Expo, 215 Brighton Ave., Boston, MA 02134; (617) 254-1445.

IBM's VLSI academic initiative

IBM's Federal System Division in Manassas, Virginia, has established a VLSI program with the University of Illinois, Pennsylvania State University, and Purdue University. This program allows universities to use IBM's Master Image chip design system and methodology. Students design 4.2 mm × 4.2 mm, 2-micron NMOS Master Image chips. Each contains 560 cell locations. This Master Image provides a sufficient area to implement nontrivial designs, but also limits the design complexity to a manageable semester project.

Students are provided with a macrocell library of predesigned functional blocks ranging from inverters to highly automated placement and wiring facilities, allowing designers to concentrate on logic design and functional verification.

The unique feature of this arrangement is the design methodology and test requirements levied on the designer.

Only a limited number of designs which pass rigorous logical, physical, and testability rule checks may subsequently be selected by the professors to be fabricated by IBM. Fabricated chips returned to the student designers are accompanied by the results of stuck fault verification testing.

Complete closure of the design process is obtained by the student designer functionally testing the chip and verifying that it performs its predicted logic function. The chips are packaged in 48-pin dual in-line packages with 43 I/O connections.

The hardware portion of the design facility is centered around an IBM 4341 computer or its equivalent. Schematics and physical layouts can be viewed on a Tektronix 618/614 storage display terminal. More information can be obtained from N. C. Panella, IBM Federal Systems Division, 9500 Godwin Dr., Manassas, VA 22110.

Intel's CMOS EPROM gets first IC mask copyright

In early January, Intel's 27C256 CMOS EPROM chip became the first chip to be registered under the new Semiconductor Chip Protection Act of 1984. Motorola, Inc., and Harris Corp. reportedly also registered a MC68020 32-bit microprocessor and a 64K PROM, respectively.

To secure protection, owners of mask works must apply for registration of their claims with the copyright office. Owners must register their works within two years after the date on which the mask work is commercially exploited, or the opportunity to gain protection under the act will be lost.

Protection for a mask work begins on the date the work is registered with the copyright office, or on the date the mask work is first commercially exploited anywhere in the world. Protection lasts for 10 years.

To apply for registration of a mask work, a completed Form MW and a nonrefundable $20 filing fee must be sent with the appropriate identifying material to Register of Copyrights, Department MW, Library of Congress, Washington, DC 20540. Form MW can be obtained free of charge by sending a request to Information Section, LM-401, Copyright Office, Library of Congress, Washington, DC 20540, or by calling the forms hotline at (202) 287-9100.

Sentry discontinues showing at Semicon West

Sentry Test Systems (previously Fairchild Component Test Systems) says that it will no longer show its products at Semicon West. Instead, Sentry will demonstrate its test systems at its own West Coast facilities. The company feels that in-house demonstrations are more effective, particularly for large, high-technology, high-pin-count systems such as the Sentry 50 VLSI and the Series 80 analog/digital test systems.

During Semicon West, Sentry will conduct an open house at its San Jose, California, facility. A broad range of memory, digital, and analog products will be on display. Visitors will also have the opportunity to preview new products and to inspect the company's engineering, research, and production facilities.

Sentry notes that it will continue to participate in Semicon technical programs and that it will exhibit products at the International Test Conference November 19-21 in Philadelphia.