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BIST allows thorough testing at reasonable cost. The chip overhead due to BIST can be minimized by a wise choice of implementation technique.

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Current designs for random logic chips use a variety of BIST architectures—from highly structured approaches for semicustom parts to mixed techniques for custom devices.

Implementing a Built-In Self-Test PLA Design  37
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By achieving high fault coverage at low overhead, this design scheme offers a practical solution to the PLA testing problem.

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Exploiting the regularity of data flow structures, this hybrid technique combines the advantages—but avoids the weaknesses—of existing BIST schemes.

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Testing, testing, testing! still shipping defective products? This method, which relates defect level and random patterns, may help you determine a sufficient test length.

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BIST started life as a mistake; it is now a key strategy. This article offers an insider's account of a decade of built-in self-test development at Motorola.

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