Guest Editor's Introduction

**Design Automation**

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The Design Automation Conference has the reputation of bringing together practitioners in a variety of disciplines who share the common goal of using the computer to perform design tasks. Correspondingly, the design field's most significant development in recent years has been the integration of individual disciplines into systems that extend throughout the design process from conception to manufacture. These systems offer benefits that are due as much to the smooth flow of information between parts of the process as they are to the new capabilities the systems themselves provide. Sophisticated workstations and computer networks play as large a role in realizing these systems as improvements in algorithm programming. Thus, concepts and innovations that originated in universities and were shared in open forums like the DAC now influence product cost and development cycles for many manufacturers.

The articles chosen for this special issue of *Design & Test* were originally presented at the 21st Design Automation Conference. Selected to represent key activities in the integration process, they illustrate the emphasis that is being placed on complete design systems and the languages used to communicate between the component parts of these systems. In addition, the quality of a design is being improved by providing enhanced tools for simulation and verification before a chip is fabricated. Lastly, they show how classical approaches to design and test are being augmented with knowledge-based systems that enable us to learn from our experience. Thus, the emphasis is on the specific design and synthesis task performed by the engineer and not on analysis tools that aid in this process.

In the past, the design community was primarily concerned with processing large amounts of data in a reasonable time so that increasingly complex VLSI chips could be designed. Now, of equal concern is rapid experimentation and a comparison of alternatives so that final product performance is improved. The effect is a shift from the automation of an initial design to the management of the change process so that alternatives can be evaluated.

The lead article, "The Magic VLSI Layout System," by John Ousterhout et al., illustrates the effect of taking an integrated approach to the design of a VLSI chip. Magic is a smart layout system for integrated circuits. The user interface combines the efficiency of mask-level design with the flexibility of symbolic representations. It provides a continuous design-rule checker that operates in the background to ensure that the changes that are made do not violate the underlying connectivity or the design rules that govern the processing technology. In addition, it provides the capability for interactively stretching and compacting the layout, routing around existing connections in channels, and hierarchical circuit extraction to verify that the correct design has been realized. The efficiency of the overall system is heavily dependent upon the data structure that was chosen to implement these operations.

The second article, "Hierarchical Layout Verification," by Todd Wagner, illustrates the importance that must be placed upon automatic verification of the correctness of a system that designs extremely complex VLSI chips. The article describes how the comparison of the schematic to layout net list is performed and how the design-rule checking is carried out. The key to the system is a hierarchical cell structure that is flexible enough to handle the complexities of VLSI design and yet takes into account the restrictions that are necessary for practical fabrication of these chips. Thus, the system verifies that a chip is manufacturable as well logically correct.

The complexity of VLSI design requires us to seek alternatives to the classical methods of analysis. The article entitled "Statistical Fault Analysis," by Sunil Jain and Vishwani Agrawal, illustrates a statistical fault analysis program that is proposed as an alternative to classical fault simulation of digital circuits. The controllability and observability of the circuit nodes are defined as probabilities that are estimated from signal statistics obtained from fault-free simulation. The computed probabilities are used to derive unbiased estimates of fault detection probabilities and overall fault coverage for a given set of vectors. It has been demonstrated that fault coverage and detected fault data obtained from Staefan agree quite favorably with fault
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Simulation results for the actual circuit.

The fourth article, "The Redesign System: A Knowledge-Based Approach to VLSI CAD," by Louis Steinberg, illustrates another approach to reducing the complexity of the design task. In this case, artificial intelligence techniques are offered as an alternative to classical synthesis approaches for VLSI; a knowledge-based approach provides an interactive aid in the functional redesign of digital circuits. The approach combines rule-based knowledge of design tactics with an ability to analyze signal propagation through the circuit to help the user focus on the appropriate portion of the circuit to redesign; it then suggests local design alternatives. The article presents data illustrating the effect of this approach on the design process and discusses directions for future work.

The integration of the various tools into a complete design system and the assembly of design systems from individual workstations requires communication between programs and between systems. The fifth article, "Towards A Standard Hardware Description Language," by Karl Lieberherr, describes the general requirements placed on hardware description languages used as input to design systems. One language is described, along with its advantages in integrating various tools used at GTE Labs. These tools include a silicon compiler that translates the circuit description into a layout. Hardware description languages provide the key to communicating our objectives to design tools; this article shows how well we have perfected such a medium.

The last paper, "EDIF: A Mechanism for the Exchange of Design Information," by John Crawford, describes the cooperative effort of several companies active in the workstation field to define a language that can be used to communicate between different vendors' components. The resulting format can act as the interface between the variety of CAE/CAD tools and foundry services that are now available to electronic engineers. It is general enough to allow the various vendors to interface to each other's systems, and it does not suffer from the limitations usually found in specialized applications. The benefits of the adoption of a standard electronic design interchange format are important and far reaching. Rather than being bound to follow a single manufacturer's product line, customers can shop among various vendors for equipment and services that best meet their needs. From a developer's point of view, it minimizes the amount of work necessary to interface to other vendors' tools and foundry capabilities.

In summary, we are proud to present six significant pieces of work that illustrate the direction that is being taken in design automation. We are tending to integrate complete systems that perform all functions efficiently upon a single set of data. These systems can be either realized entirely within a single design organization or assembled from vendor tools. To be efficient, the designer must either rely upon design rules or design verification to ensure that the correct performance can be realized, and upon simulation or simulation alternatives to verify that the design performs correctly and is testable. Lastly, to take advantage of the variety of tools that are available, hierarchical design languages and interface formats are necessary, and progress is being made in these areas.

Lawrence A. O'Neill is head of the Integrated Manufacturing Development Department at AT&T Bell Laboratories. His current responsibility is the optimization of the product realization process from the acquisition of design information through the control of manufacturing equipment. Previously he developed a user-friendly computer-aided engineering system that improved the efficiency of the design engineers. He is particularly concerned with application of software engineering to provide maintainable and modifiable systems. He received a BSEE from the University of Maryland, an MEE from the Catholic University of America and a PhD in electrical engineering from Johns Hopkins University.

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