Is LASAR logic simulation best?
Take this test.

1. A logic simulator for LSI circuits must accurately model:
   A. Tristate and bidirectional gates
   B. Timing characteristics of primitives and device models
   C. MOS charge retention and current drive capability
   D. All of the above

2. Timing verification can be best achieved by a simulator that has:
   A. Min/max timing analysis
   B. Common ambiguity resolution
   C. Accurate hazard reporting
   D. All of the above

3. Engineering productivity will be greatest when a simulator has:
   A. A comprehensive library of primitives and device models
   B. Fault simulation to uncover testability problems and trace faults
   C. Links to CAD workstations and testers
   D. All of the above

If you answered D. for each question, you'd be right. And only one simulator can give you all of the above.
LASAR™ Version 6 by Teradyne.
Why settle for second-best when you can have LASAR today? LASAR software predicts logic states and event timing more accurately than any other simulator.
Now it's easier to create high-quality designs for VLSI devices and boards than ever before. Here's how.

Our logic is flawless.
Designers using LASAR software can simulate logic activity more accurately than with any other tool available. Regardless of circuit complexity or IC technology.
LASAR algorithms let you completely simulate tristate and MOS activity to evaluate buses and wired net behavior. You'll have more confidence in your simulation results. And you'll eliminate multiple prototype iterations.

Our timing is perfect.
LASAR software gives engineers the only worst-case timing analysis that really works. You can make sure that circuits function repeatably. Under all operating conditions, with mixed component sources or different device lots.
The simulator correctly evaluates circuit timing, including minimum/maximum propagation...
delays, and timing constraints at device inputs. And you won't have to deal with reams of false hazard reports. Or miss any real hazards. By eliminating common ambiguity—the skew in signal timing shared by reconverging signals—LASAR Version 6 pinpoints all actual timing hazards. You'll verify designs more efficiently than ever before.

A model simulator.
Transfer the details of your design directly from your schematic capture or layout system. Or use LASAR Version 6 to model devices from the bottom up, using logic, memory and MOS primitives or gate array macros.
You can also build from the top down using Teradyne Modeling Language. TML is a register transfer language program that lets you compile a structural model from a functional description of a device.
For board-level modeling, LASAR Version 6 offers the largest, most accurate device library available, with more than 3,800 devices, SSI to VLSI.
You'll be able to create complete board models more efficiently than with any other simulator.

Testing with the right connections.
Today more people use LASAR for test program generation than any other simulator.
Using the same simulator for design and test, you can typically save months of work. There's no need to remodel devices, recreate the net list or rewrite patterns.
Efficient time-based fault coverage analysis lets you know that circuits are testable. It gives test engineers confidence in the quality of their test programs. While pinpointing areas that need more work.
To make the design-test link easier, LASAR software takes into account tester behavior such as driver skew, and pattern timing and control characteristics.
By creating links to high speed testers, prototype and production test plans can be ready faster, reducing time to market.

How can you improve your grade?
Whether or not you scored well on our test, you now have enough information to make a very intelligent decision. Contact Teradyne today.
Write Teradyne, 321 Harrison Avenue, Boston, MA 02118. Or call Daryl Layzer, LASAR Software Product Group, 617-482-2700, ext. 2808.