Content addressable memory (CAM) plays an important role in computer architecture, but architects have been unable to use it as widely as they would like because of its major disadvantage when compared to RAM—conventional NOR CMOS CAM is highly, and even prohibitively, power hungry.

In “Resistive Address Decoder” (IEEE Computer Architecture Letters, vol. 16, no. 2, 2017, pp. 141–144), authors Leonid Yavits, Uri Weiser, and Ran Ginosar propose a new CAM design—the resistive address decoder—that makes CAM power usage comparable to that of RAM and thus opens the door to much greater use of CAM.

Consider a typical NAND address decoder, where the address of a memory row is hardwired by connecting either address bit line or inverse bit line to the gate of an NMOS transistor. In a row where the address matches the hardwired pattern, all NMOS transistors are turned on and the row is selected. The authors add two resistive elements, such as memristors or spin-torque transfer magnetic RAM, to each NMOS transistor in a voltage-dividing manner (see Figure 1). Memristors are two-terminal devices whose resistance is changed by the electrical current. The resistance of the memristor typically has two states: \( R_{\text{ON}} \) (low resistive state) and \( R_{\text{OFF}} \) (high resistive state). By programming the left memristor of a bit cell to \( R_{\text{ON}} \) and the right one to \( R_{\text{OFF}} \), the NMOS transistor gate is effectively connected to the address bit line. Conversely, by programming the left memristor to \( R_{\text{OFF}} \) while programming the right one to \( R_{\text{ON}} \), the NMOS transistor gate is effectively connected to the inverse address bit line. The additional transistor in a bit cell is used to program the memristors. Such an approach achieves a two-fold effect: the address pattern in each row becomes programmable rather than hardwired, and the memristor pair forms an XOR gate, allowing comparison of the input address bit to the bit “programmed” into the resistive elements. These effects enable content addressability, effectively turning an address decoder into CAM.
The authors’ experimental results are quite promising. They show that the programmable resistive address decoder’s energy and timing overheads are nonexistent during memory read and negligible during memory write. The area overhead is also minimal.

There are many possible applications of low-power CAM. Within contemporary processor cores, various storage structures are currently less than fully associative, including caches and translation look-aside buffers. If their hardwired address decoders are replaced with the programmable resistive address decoders, these structures become fully associative at the timing and energy cost of direct mapped ones.

Another intriguing application of low-power CAM is a virtually addressable main memory, which is enabled by replacing the hardwired NAND address decoder of main memory with the programmable resistive address decoder. Virtually addressable memory might significantly increase the CPU performance when running virtual machines and hypervisors (where nested memory mapping is required), as well as improve memory performance and utilization (by reducing the physical memory fragmentation), and enhance the system security.

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