For more than 65 years, IEEE Transactions on Computers (TC) has served the computing community with top-quality research contributions. We recently played a stimulating game: we rolled back 10+ years, grabbed a few TC issues, looked at the state of the art in a particular field, compared it with today’s picture, and reflected on the fact that “old” problems have been solved and “new” questions have emerged. First, there was Moore’s law. Then came Dennard scaling (DS), which states that when moving from one technology node to the next, a transistor’s power density is constant—that is, independent of the technology. Recently, DS was discontinued. So, what will happen in the future?

It’s a fact that power density will be a major challenge for the foreseeable future. Despite orders-of-magnitude improved efficiency, power consumption per area is sharply rising. The reason is that, after a long reign, DS has ended because supply voltage has stopped scaling down. Some refer to this problem as “dark silicon,” inferring that major parts of a chip would need to remain idle (dark)—but expensive, highly integrated silicon clearly can’t stay idle.

One promising solution is to tightly control power densities, operating close to or even temporarily exceeding recommended densities. To investigate the physical implications of high power densities, we must distinguish among peak and average temperatures and temporal and spatial thermal gradients because they trigger circuit-aging mechanisms such as negative-bias temperature instability and electromigration.

Various techniques have been investigated to mitigate, for example, reconfigurable circuits’ aging problem.1 System-level approaches can also mitigate the problem at the OS level, where hardware resources are carefully selected to avoid rapid circuit degradation.2 More accurate circuit-aging models are needed to allow high-level methods to operate on-chip systems at their real power-density limits (rather than costly conservative ones),3 while continuously monitoring the tradeoff between performance and thermally triggered aging mechanisms and their negative short- and long-term reliability effects.3 Involving all abstraction layers in the on-chip system’s design process in this smart way will help extend DS. The key is cross-layer approaches.4

REFERENCES

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