A new chipmaking approach marks the biggest change in transistor technology since the introduction of polysilicon-gate, metal-oxide-semiconductor transistors in the late 1960s, according to Intel cofounder and chair emeritus Gordon Moore.

This is how the man for whom Moore’s law was named evaluates a move by three major chipmakers—Advanced Micro Devices (AMD) and IBM working together, and Intel on its own—to change two of the three most important materials used to make the transistors that are at the heart of today’s microprocessors.

This could overcome the most substantial roadblock to continuing to use current production processes to shrink transistor elements and thereby increase energy efficiency and continue to use current chipmaking techniques, thereby avoiding expensive fabrication-plant changes.

Until now, as transistors have gotten smaller, they have faced potential current-flow problems. Also, the transistors’ insulation layers have gotten so narrow—as little as five atoms thick—that they leak enough electrons to increase power consumption, generate heat, and hurt performance.

Further thinning the insulator layer—called the transistor gate dielectric—to three atomic layers, to continue shrinking transistors, would make this worse, noted Risto Puhakka, president of VLSI Research, a chip-market analysis firm.

Use of the new materials, on the other hand, reduces leakage five to 10 times from current levels, said Bohr.

The new chips could be used in laptops, PCs, and servers, and, because of their energy efficiency, eventually even in power-constrained devices like cell phones.

The technology faces potential challenges such as production complexity and the increased risk of material contamination.

Nonetheless, Intel plans to mass-produce chips with 45-nm feature sizes using the new materials during the second half of this year, said Bohr.

IBM expects to begin producing 45-nm chips based on the materials next year.

“If you are going to move to more advanced processor technology, you will have to consider this approach as one of the most likely options,” said Jim McGregor, market-research firm InStat’s director for semiconductors and enabling technologies.

A NEW DAY

Electrical current flowing at either a high or low level across two gate electrodes on either side of the transistor channel represents the ones and zeros of binary data.

The insulating gate dielectric, traditionally made of silicon dioxide, sits below the gate electrode and above the silicon substrate. It transmits voltage from the gate electrode to the underlying transistor channel and prevents the leakage of current when the electrode is powered.

As chipmakers make transistors smaller so that they can pack more of them onto chips, they have made the gate dielectric thinner. However, this has led to dramatically higher gate leakage and power consumption.

“Leakage has been an issue for the last couple of generations of processors, starting at those with 130-nm [feature sizes],” McGregor noted.

The technology

The AMD, IBM, and Intel chipmaking approaches focus on using new materials in the gate dielectric. Different materials must also be used in the gate electrodes so that they can function optimally with the new dielectric.
**Gate dielectric.** As Figure 1 shows, the gate dielectric traditionally has been made of silicon dioxide, a poor conductor of electricity that prevents the leakage of electrons from the gate to the substrate. Over time, Intel has reduced the silicon-dioxide gate dielectric’s thickness to 1.2 nm—five atomic layers—for chips with 65-nm feature sizes.

However, electrons increasingly leak through such a thin layer. This wastes energy. And, when the electron flow hits the dielectric, the resistance generates heat.

To cope with these problems, AMD, IBM, and Intel have experimented with making gate dielectrics using high-k materials, including hafnium. (“k” represents the dielectric constant, which describes a material’s ability to transmit charge when a voltage is applied.)

Jim Hutchby, director of device sciences at Semiconductor Research Corp., an industry research-management consortium, said AMD, IBM, and Intel probably are using nitride of hafnium silicate consisting of hafnium, silicon, oxygen, and nitrogen. However, AMD, IBM, and Intel are not disclosing the exact mix of materials used in their new designs.

As transistors have become smaller horizontally, they have also had to cope with narrower transistor channels. To provide the current necessary for the system to accurately read high and low levels, the smaller systems must get more electrostatic charge through the dielectric layer to the channel.

High-k materials can transmit more charge than silicon dioxide. And building the dielectric thicker vertically would provide more resistance, which reduces leakage without making transistors bigger horizontally.

Scientists have researched the use of high-k materials in transistors for about two decades, noted UC Berkeley’s Subramanian. However, the material decreased performance by reducing the ability of electrons in the channel to move around and thereby increase current flow through the channel.

Researchers minimized this problem by adding an intervening layer of silicon oxide. The material reduced the effect of thermal currents between the transistor channel and the dielectric, which inhibit electron mobility.

**Gates.** Transistor gates currently are made of layers of polysilicon—doped noncrystallized silicon—deposited onto the substrate.

High-k dielectrics can’t be used with conventional polysilicon gate electrodes because the two materials don’t match well electromagnetically. This keeps the current flow across the transistor channel from switching as quickly as necessary.

To cope with this, AMD, IBM, and Intel have developed metal gate electrodes, which match better electromagnetically with the high-k materials.

**Intel**

Intel has developed a prototype 45-nm static RAM chip. The company has also demonstrated prototypes of 45-nm microprocessors, code-named Penryn, that will use the new technology. Intel plans to begin mass-producing and releasing them later this year. These chips will be the next-generation Core 2 Duo, Core 2 Quad, and Xeon families of mobile, desktop, and server multicore processors.

Intel anticipates the first generation of the new 45-nm chips will provide twice the transistor density of current 65-nm processors, said company spokesperson Kari Aakre.

They will also reduce gate oxide leakage by 90 percent, consume 30 percent less transistor-switching power, and either decrease source-to-drain leakage by 80 percent or offer 20 percent more transistor-switching speed.

To improve precision, Intel says, it will build the dielectric using atomic-layer deposition, in which a machine deposits the high-k material one layer of atoms at a time.

The company will use traditional dry lithography to build the 45-nm chips. However, it is considering immersion lithography for the next generation of chips, which will have 32-nm feature sizes. This technique focuses the light that etches the circuit pattern onto the wafer through a thin layer of water. This helps better focus the light and thereby achieve smaller features.

**IBM and AMD**

IBM and AMD are working with Sony and Toshiba on their chipmaking project.
IBM is adding the infrastructure necessary to build the new chips into its semiconductor-manufacturing line in East Fishkill, New York. The company plans to introduce the new technology in 45-nm chips next year but has not disclosed the types of computers or devices in which the processors will be used.

The company has been working on the technology for nearly a decade and had to overcome significant manufacturing and materials challenges to create a reliable, mass-produced product, said IBM Research senior manager Mukesh Khare.

For example, identifying compatible high-k-dielectric and metal-gate-electrode materials was difficult, as was identifying metals that could endure the necessary high-temperature manufacturing process, explained Ghavam Shahidi, director of silicon technology at IBM’s Thomas J. Watson Research Center.

He said the company’s high-k chips will reduce gate leakage by 99.9 percent and improve performance by up to 20 percent.

AMD and IBM plan to build the new chips using immersion lithography.

AMD is not sure whether it will incorporate the new technology into its 45-nm or 32-nm chips, said Jon Carvil, the company’s technology communications director. It is not clear whether the benefits are compelling enough for use in 45-nm processors, he explained.

CHIPMAKING CHALLENGES

Even though the new technique uses current chipmaking processes, retooling existing fabrication plants will still be expensive, noted VLSI Research’s Puhakka.

Raj Jammy, director of the Front End Processes Division at Sematech, a chip-industry research consortium, noted that for 30 years, the industry has created gate dielectrics by subjecting parts of the chip substrate to oxygen exposed through a photomask. This oxidation process yields the dielectric’s silicon oxide.

Chipmakers have not figured out how to use this type of process with high-k materials and instead have to deposit material directly onto the substrate. The deposition process entails the risk of material contamination.

Also, Jammy said, the AMD, IBM, and Intel chips will introduce two new sets of materials and immersion lithography into the production process. Such a big change could prove to be complex and difficult.

For example, ensuring reliability and putting the new materials into the process flow will be a challenge, noted Intel’s Bohr.

All new high-performance processors will use the new materials within the next five years, predicted Jammy.

However, said VLSI Research’s Puhakka, the up-front capital investment necessary to build new facilities or convert current ones to produce the new processors won’t make sense for manufacturers of chips that don’t need high performance or that are likely to be produced only in small quantities.

While the new gate and dielectric materials are important, McGregor said, advances in design and lithography techniques will have to occur to enable the ongoing manufacture of higher-performance processors using current chipmaking techniques.

And, said University of Texas associate professor Steve Keckler, many real advances are likely to come not from new materials but from the development of better multicore chips—which improve performance by having multiple cores run tasks in parallel rather than by increasing clock speed—as well as from the optimization of applications for these processors.

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