As Wi-Fi networks have become increasingly popular, many corporations have added Wi-Fi access to give employees easier access to corporate data and services. Although IT personnel control Wi-Fi access points in the corporate network, they cannot control access points in home networks. These networks thus give hackers new opportunities to gain unauthorized access to corporate computer systems and their data.

The results of an investigation conducted to assess the security level in Wi-Fi networks in Bergen, Norway, provide a context for analyzing some popular wireless security techniques and for offering suggestions on how to better protect these networks from hacking.

Parallelism and the ARM Instruction Set Architecture
pp. 42-50

John Goodacre and Andrew N. Sloss

The ARM reduced-instruction-set computing processor has evolved to offer a family of chips that range up to a full-blown multiprocessor. Embedded applications’ demand for increasing levels of performance and the added efficiency of key new technologies have driven the ARM architecture’s evolution.

The ARM team has used the full range of computer architecture techniques for exploiting parallelism, including variable execution time, subword parallelism, DSP-like operations, thread-level parallelism and exception handling, and multiprocessing.

The ARM architecture’s developmental history shows how processors have used different types of parallelism over time. With its foundation in low-power design, the new ARM11 MPCore multiprocessor can bring low power to high-performance designs, which show the potential to truly change how people access technology.

Configurable Processors: A New Era in Chip Design
pp. 51-59

Steve Leibson and James Kim

Designers can use advanced development tools to tailor a microprocessor core for specific application tasks and generate the processor’s register-transfer-level description. They can also generate all the requisite software-development tools for that architecture in minutes. This entire process takes a shockingly brief time relative to the time spent designing processors and their associated development tools in prior eras.

With automated tools, designers can focus on system architectural issues to achieve performance goals rather than spending time designing individual functional blocks within the SoC.

The configurable processor represents the next evolutionary step in microprocessor development, paving the way for new and interesting architectures that employ multiple, heterogeneous processor cores and exploit the qualities of advanced semiconductor lithography.

An Open Platform for Developing Multiprocessor SoCs
pp. 60-67

Mario Díaz Nava, Patrick Blouet, Philippe Teninge, Marcello Coppola, Tarek Ben-Ismail, Samuel Picchiottino, and Robin Wilson

The opportunities that nanometer technologies provide, combined with the consolidation of platform-based design approaches, have driven the evolution toward multiprocessor architectures, and the network-on-chip paradigm suggests new methods for designing and verifying embedded systems.

Clearly, a pure software simulation platform can’t provide the performance required for developing multiprocessor system-on-chip designs. What’s more, a main design risk for today’s systems is the architecture, which developers must validate early in the design cycle because it has the biggest impact on system dimensioning and performances.

The authors describe an approach that introduces concurrent hardware and software engineering early in the development process and uses low-cost emulation facilities. Their approach extends the emulation used for verifying application-specific integrated circuits and application-specific standard product devices to multiprocessor architectures. They plan to introduce this platform in consumer and telecommunications product development to increase software and hardware engineers’ productivity, which will reduce development time and costs while ensuring design and product quality.

Evaluating Digital Entertainment System Performance
pp. 68-72

Markus Levy

Digital entertainment systems have become the driving force behind the expansion of the semiconductor market, outstripping even PCs. In 2003, for example, smart phones represented about 3 percent of the 500 million mobile phones sold worldwide, with analysts expecting their sales to grow at triple-digit year-over-year rates.

More than half of the 600 million mobile phones sold in 2004 included a color display and digital camera. The implementation of more advanced features such as accelerated 2D and 3D graphics, videoconferencing, mobile multimedia, and games has raised performance requirements. The same holds true for other digital entertainment devices.

Rapid advances in semiconductor technology, microarchitectures, and embedded systems have made the adoption of these features possible. As a result, software complexity will continue to increase to keep pace with overall system complexities.

Performance and quality provide good starting points for evaluating a digital entertainment system, but energy consumption is an equally important metric.