Monday, October 5

Tutorial Registration
Tutorial I: Cache Memories, Alan Smith, U. C. Berkeley
Survey of design considerations for cache memories including recent material on cache workloads, cache miss ratios, and cache consistency algorithms.

Tutorial II: RISC Architectures: Principles & Examples, John Hennessy, Stanford University
Survey of the principles behind the RISC approach using research and commercial machines to illustrate design tradeoffs.

Tuesday, October 6

Conference Registration
Keynote Speaker: Niklaus Wirth, ETH

Session I: Operating Systems, Chair: Forest Baskett, Silicon Graphics
“VLSI Assist in Building a Multiprocessor Operating System,” B. Beck, B. Kasten, S. Thakkar, Sequent Computer Systems

Session II: Languages and Instruction Sets, Chair: Chuck Thacker, DEC Systems Research Lab
“Tags and Type Checking in LISP: Hardware and Software Approaches,” P. Steenkiste, J. Hennessy, Stanford University
“The Effect of Instruction Set Complexity on Program Size and Memory Performance,” J. Davidson, R. Vaughn, U. of Virginia
“The DRAGON CPU,” E. McCreeght, Xerox Palo Alto Research Center

Session III: Miscellaneous Architectural Support, Chair: David Ditzel, AT&T Bell Labs
“Coherency for Multiprocessor Virtual Address Caches,” J. Goodman, U. of Wisconsin
“Cheap Hardware Support for Software Debugging And Profiling,” T. Cargill, B. Locanthi, AT&T Bell Labs
“An Experimental Coprocessor for Implementing Persistent Objects on an IBM 4381,” C. Georgiou, S. Palmer, P. Rosenfeld, IBM T. J. Watson Research Center

Wednesday, October 7

Session IV: Compilers I, Chair: John Hennessy, Stanford University
“Integer Multiplication and Division on the HP Precision Architecture,” D. Magenheimer, L. Peters, K. Pettis, D. Zuras, Hewlett-Packard
“The Mahler Experience: Using an Intermediate Language as a Machine Description,” D. Wall, DEC Western Research Lab
“A Study of Scalar Compilation Techniques for Pipelined Supercomputers,” S. Weiss, J. E. Smith, MCC

Session V: Compilers II, Chair: Steve Muchnick, SUN Microsystems
“Compiling Smalltalk-80 to a RISC,” W. Bush, A. Samples, D. Ungar, P. Hilfinger, U. C. Berkeley
“Superoptimizer — A Look at the Smallest Program,” H. Massalin, Columbia University

Session VI: Functional & Logic Languages, Chair: Randy Katz, U. C. Berkeley
“RISCs or CISCs for Prolog: A Case Study,” G. Borriello, A. Chersonen, P. Danzig, M. Nelson, U. C. Berkeley
“A RISC Architecture for Symbolic Computation,” R. B. Kieburz, Oregon Graduate Center

Session VII: New Machines I, Chair: Jim Goodman, U. of Wisconsin
“Design Tradeoffs to Support the C Programming Language in the CRISP Microprocessor,” D. Ditzel, H.
McLellan, A. Berenbaum, AT&T Bell Labs
"Firefly: A Multiprocessor Workstation," C. Thacker, L. Stewart, DEC Systems Research Center
"Pipelining and Performance in the VAX 8800," D. Clark, DEC

Thursday, October 8

Session VIII: New Machines II, Chair: E. M. McCreight, XEROX Palo Alto Research Center
Panel Session: Lies, Damned Lies, and Benchmarks, Organizer: Alan Smith, U. C. Berkeley

Conference Chairmen

General: Martin Freeman Stanford University
Program: Randy Katz U.C. Berkeley
Finance: Dennis Reinhardt DAIR Computer Systems
Publicity: Jim Flournoy Consultant

Program Committee

Randy Katz U.C. Berkeley (chairman)
Forest Baskett Silicon Graphics
David Ditzel AT&T Bell Labs
James Goodman U. of Wisconsin
John Hennessy Stanford University
Edward McCreight Xerox PARC
Steven Muchnick Sun Microsystems
Richard Sites DEC Hudson
Alan Smith U.C. Berkeley
Chuck Thacker DEC Systems Res. Center
Philip Treleaven University College London
Mario Tokoro Keio University

Registration

Conference registration includes one copy of the proceedings, lunches, breaks, etc. Tutorial registration covers both tutorials and includes one copy of notes for each tutorial, a lunch, and breaks. Student registration does not include meals. For further information, contact Martin Freeman (415) 725-3633.