12 Guest Editors’ Introduction: Systolic Arrays—From Concept to Implementation
José A.B. Fortes and Benjamin W. Wah
Systolic arrays have regular and modular structures that match the computational requirements of many algorithms. Their implementation requires that a wealth of subsumed concepts and engineering solutions be mastered and understood.

18 Wavefront Array Processors—Concept to Implementation
Most signal and image processing algorithms can be decomposed into computational wavefronts that can be processed on pipelined arrays.

35 The Saxpy Matrix-1: A General-Purpose Systolic Computer
David E. Fousser and Robert Schreiber
The Matrix-1 employs a programmable and reconfigurable systolic array that achieves nearly gigaflop performance for problems in signal processing and matrix computation.

45 SLAPP: A Systolic Linear Algebra Parallel Processor
Barry L. Drake, Franklin T. Luk, Jeffrey M. Speiser, and Jerome J. Symanski
Recent signal-processing algorithm developments have stressed direct methods that operate on the data matrix via orthogonal matrix decompositions. Systolic arrays appear to be quite well matched to the requirement for real-time computation of these algorithms.

51 Some Systolic Array Developments in the United Kingdom
John V. McCanny and John G. McWhirter
Two major UK systolic array projects are described. The first concerns development of a wavefront array processor for adaptive beamforming, the second the design of novel high-performance signal-processing chips.

65 Fault Tolerance Techniques for Systolic Arrays
Jacob A. Abraham, Prithviraj Banerjee, Chien-Yi Chen, W. Kent Fuchs, Si-Yen Kuo, and A.L. Narasimha Reddy
This article describes various techniques for fault tolerance that can be applied to systolic array architectures. The approach of algorithm-based fault tolerance is shown to be the natural one for such systems.

77 Partitioning: An Essential Step in Mapping Algorithms Into Systolic Array Processors
Juan J. Navarro, José M. Llaberia, and Mateo Valero
The efficient solution of a large problem on a small systolic array requires good partitioning techniques to split the problem into subproblems that fit the array size.

91 Systolic Arrays: A Survey of Seven Projects
This special section provides a concise overview of seven projects concerned with the design and implementation of systolic arrays.
On the cover
Guest editors José Fortes and Benjamin Wah point out that systolic arrays are so called because analogies can be drawn between their architecture and that of the human circulatory system. The human heart sends and receives a large amount of blood as a result of the frequent and rhythmic pumping of small amounts of that fluid through the arteries and veins. In this analogy, the heart corresponds to the source and destination of data (such as a global memory), and the network of veins is equivalent to the array of processors and links. Another analogy is that in many of the first proposed systolic architectures, processing elements alternated between cycles of “admission” and “expulsion” of data—much in the same way that the heart behaves with respect to the pumping of blood.

Cover image: Benn Mitchell © Image Bank West
Cover design: Jay Simpson

In the next issue
CAD-based robot vision

Career Opportunities 118, Advertiser/Product Index 136, Reader Service Card 136A, Change-of-Address Form 111, Membership Application 11

DEPARTMENTS

6 President’s Message
7 Letters to the Editor
104 Open Channel
106 Standards
108 Update
110 Computer Society News
112 Conferences
113 Call for Papers
115 Calendar
120 New Products
127 Microsystem Announcements
128 IC Announcements
129 Computer Society Officers and Information
130 Roster of Computer Society Committees
133 Book Reviews
135 New Literature

On the cover
Guest editors José Fortes and Benjamin Wah point out that systolic arrays are so called because analogies can be drawn between their architecture and that of the human circulatory system. The human heart sends and receives a large amount of blood as a result of the frequent and rhythmic pumping of small amounts of that fluid through the arteries and veins. In this analogy, the heart corresponds to the source and destination of data (such as a global memory), and the network of veins is equivalent to the array of processors and links. Another analogy is that in many of the first proposed systolic architectures, processing elements alternated between cycles of “admission” and “expulsion” of data—much in the same way that the heart behaves with respect to the pumping of blood.

Cover image: Benn Mitchell © Image Bank West
Cover design: Jay Simpson

In the next issue
CAD-based robot vision