TUESDAY, JUNE 3

1: Opening
"Welcome Address", H. Aiso, Conference Chairman, Keio U
"Featured Speaker", Eichi Goto, U of Tokyo

2-A: Parallel AI-Architectures
Chair: D. DeGroot, Quentin, M. Kitagawa, U of Tokyo
"A Mobile Architecture for a Relational Knowledge Base", H. Yokota, IIT, Japan
"Implementation and Evaluation of a List-Processing Oriented Dataflow Machine", M. Amazami, M. Takeo, R. Hasegawa, H. Mikami, NTT, Japan
"A New String-Search Hardware Architecture for VLSI!", K. Terasaka, H. Nakagawa, NTT, Japan
"Parallel Algorithms and Architectures for Rule-Based Systems", A. Gupta, C. Forgy, R. Wegid, CMU, USA

2-B: Multiprocessor Performance Analysis
Chair: R.S. Davidson, U of Illinois, T. Yoda, STL
"Concept: Design of a Multiprocessor Development System", R.H. Halstead, Jr., T.I. Anderson, R.B. Osborne, T.I. Sterling, MIT, USA
"Memory Requirements for Balanced Computer Architectures", H.T. Kung, CMU, USA
"Partitioning Programs to Enhance Concurrency in Static Dataflow Architectures", Y.C. Hsueh, T.H. Payne, L.B. Ferguson, UC Riverside, USA
"Software Implementation of a Recursive Fault Tolerance Algorithm on a Network of Computers", P. agrawal, R. Agrawal, Bell Lab, USA

3-A: AI-Architectures
Chair: J.R. Gurd, U Manchester, T. Fujisaki, IBM Japan
"Microprogrammable Processor for Object-Oriented Architecture", T. Nogiri, K. Sakoda, S. Kawasaki, Higashi, Japan
"An Instruction Fetch Unit for a Graph-Reduction Machine", S.S. Thakkar, Oregon Graduate Center, W.E. Hostmann, Hewlett Packard, USA
"Past Object-Oriented Procedure Calls: Lessons from Intel 432", F.F. Gehring, North Carolina State U, R.P. Colwell, Multiflow, Computer, USA

3-B: Performance Analysis
Chair: D. Clark, Digital, A. Sekino, NEC
"On Coupling Many Small Systems for Transaction Processing", D.M. Dias, B.R. Iyer, P.B. Yu, IBM Research, USA

4: Panel: Parallelism - Are We Still Interested?
Moderator: M. Takuro, Keio U

WEDNESDAY, JUNE 4

5-A: Parallel Prolog Architectures
Chair: J-C Syre, ERCOM, M. Yokota, IICT
"Experimentsing with EPILOG: Some Results and Preliminary Conclusions", M.I. Whis, U of New South Wales, Australia
"A Unification Processor Based on the Semi-Syntactic Array with a Broadcast Bus", Y. Shobatake, B. Also, Keio U, Japan
"The Architecture and Experimental Results of the Experimental Parallel-Inference Machine PDM-D", N. Ito, M. Sato, IICT, M. Kashi, E. Kunu, K. Kurosawa, Obi, Japan

5-B: Interconnections
Chair: J. Emer, Digital, H. Yamasaki, Obi
"An Efficient Routing Control Unit for the Sigma Network: E admired", A. Senec, IRISA, France
"The Extra-Stage Gamma Network", K.Y. Lee, W. Begazy, Oak Stad II, USA

6-A: Lisp Machines
Chair: P. Treleaven, U of Reading, T. Shimada, ETL
"Evaluation of the PACOM ALPHA: LISP Machine", M. Valhama, A. Haitor, M. Nawa, M. Kikimoto, H. Hayashi, Fujitsu, Lab, Japan
"Evaluation of the SPUR Lisp Architecture", G.S. Taylor, P.N. Hingiuer, J.R. Lucas, B.G. Zora, D.A. Patterson, UC Berkeley, USA

6-B: Special Purpose Architectures
Chair: H.T. Kung, CMU, K. Ohmori, Hosei U
"A Processor for Symbolic Instruction Execution", H. Yamauchi, M. Aoki, R. Nakamura, NTT, Japan
"Exploiting Parallelism in a Switch-Level Simulation Machine", E.F. Frank, Austel Microsystems, Australia
"Custom Hardware Accelerators", T. Anthanarath, R. Biesiada, CMU, USA

THURSDAY, JUNE 5

7-A: Dataflow Architectures
Chair: Arrivo, MIT, M. Amazami, NTT
"Evaluation of a Prototype Dataflow Processor of the SIGMA-1 for Scientific Computations", T. Shimada, K. Hiraki, K. Nishida, S. Sekiguchi, ETL, Japan

7-B: FP Architectures
Chair: P. Kogge, IBM, Y. Murooka, Weeda U
"AF-*=(0 (Log A));", Y. Shigei, T. Tobu, Japan

8-A: CPU Architectures
Chair: D. Dietz, Bell Lab, N. Koike, NEC
"VLSI-Oriented Asynchronous Architecture", M. Hirayama, Mitsubishi, Japan
"HPSn, a High Performance Restricted Dataflow Architecture Having Minimal Functional", W.M. Hwa, Y.N. Patt, Berkeley, USA

8-B: Matrix Computation Architectures
Chair: J.E. Smith, U of Wisconsin, T. Ida, IPOR
"A Computer Architecture for Dynamic Finite-Element Analysis", L.M. Napolitano Jr., Sanda National Lab, USA
"Performance Evaluation of Vector Accesses in Parallel Memories Using a Skewed-Storage Scheme", D.T. Harper, III, J.R. Jump, Rice U, USA

9-A: Image-Processing Architectures
Chair: W. Handler, U U of Nebraska, Y. Hodaka, Toshiba
"Pseudo MIMD Array Processor-AAP2", T. Kondo, T. Tsukiyama, K. Sugiyama, K. Kinuma, T. Nakashima, NTT, Japan
"Scan-Line Array Processors for Image Computation", A.I. Fisher, CMU, USA

9-B: Cache Memory
Chair: J. Hennessy, Stanford U, H. Hayashi, Fujitsu
"Software-Controlled Caches in the Nebula Multiprocessor", D.R. Cheriton, G.A. Slavenburg, P.D. Boyle, Stanford U, USA
"On the Use of Registers vs. Caches to Increase Memory Traffic", J.R. Goodman, W.G. Hau, U of Wisconsin, USA

10-A: Pipeline Architectures
Chair: T. Agerwala, IBM Research, S. Tomita, Kyoto U
"Highly Concurrent Scalar Processors", P.Y.T. Biss, E.S. Davidson, U of Illinois, USA
"Reducing the Cost of Branches", S. McFarling, J. Hennessy, Stanford U, USA
"Optimal Pipelining in Supercomputers", S.R. Kunkel, J.E. Smith, U of Wisconsin, USA

10-B: Cache Coherence
Chair: R.H. Katz, UC Berkeley, A. Fussoaka, Mitsubishi
"A Cache-Coherence Mechanism for Backplane Buses", A.J. Smith, UC Berkeley, P. Sweaney, Tateson, USA
"Multiprocessor Caches: Caches for Synchronization and Busy-Wait Locking, Waiting and Unlocking", P. Blar, A.M. Despain, UC Berkeley, USA
"Memory-Access Buffering in Shared-Memory Multiprocessor Systems", M. Dubois, C. Scheurich, USC, B. Briggs, Rice U, USA

11-Panel: AI and Scientific Computers - Are They Incompatible?
Moderator: H. Stone, IBM Research
CONFERENCE INFORMATION

Location
The 1986 International Symposium on Computer Architecture will be held at the Prince Hotel located in the Tokyo Metropolitan Area. The registration will be held at Chinzan-so restaurant which has a beautiful Japanese garden.

From New Tokyo International Airport it takes about two hours by bus to the Prince Hotel.

Conference attendees may obtain special rates by phoning Northwest Airlines Meeting and Convention Services: 1-800-322-7747. Rates as low as $227 West Coast/Tokyo round trip, no minimum stay, are available.

Tutorial
The symposium will present a full-day tutorial on June 2 on Japan’s National Project in Computer Science and Technology. Research endeavors for new computer technology promoted and supported by the Japanese Government will be presented. The four consecutive sessions are: Overview of Japanese National Project in Information Technology by H. Aiso of Keio University, Supercomputer Project by T. Yuba and T. Shimada of the Electrotechnical Laboratory, Three-dimensional Integration Project by A. Kokubu of ETL, and Fifth Generation Computer Systems Project by S. Uchida and M. Yokota of ICOT.

Technical Visits
Several research institutes and companies may offer open houses for the participants during the symposium. The open houses are currently scheduled for Thursday (pm) and Friday. Details and an application form will be available at the registration desk. Participation will be on a first-come first-service basis.

Registration
Conference registration includes one copy of the Proceedings and the reception on Wednesday. Student registration does not include the reception. To receive a discount, a student must be IEEE-CS, ACM or IPSJ Student Member. Students and participants’ spouses will be welcome at the reception for an additional fee of 10,000 yen.

Others
The official language of this symposium is English.

For further information, please write or call:

Secretariat-ISCA’86
Business Center for Academic Societies Japan
Yamazaki Bldg. 4F, 2-40-14 Hongo
Bunkyo-ku, Tokyo 113, Japan
Phone: (03)817-8831, Telex: 0722266 BCJSJ P J

Hotel Accommodations
All inquiries and applications concerning hotel accommodation shall be directed to:

Japan Travel Bureau Inc. (JTB)
Foreign Tourist Div., (CD6-7401-86)
1-13-1, Nihombashi, Chuo-ku, Tokyo 103, Japan
Phone: (03)376-7881, Telex: 24418 TOURIST J

ISCA’86 Advance Registration Form

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ACM, IEEE-CS or IPSJ Membership Number:  

(For May 6) | Member | Non-member | Student |
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Grand total: (in Japanese yen)  

Note: No personal check is accepted. All payments should be in Japanese yen.

- Enclosed is a bank draft payable to ISCA’86.
- Remitted on (date) through (name of your bank):

ISCA’86 Hotel Reservation Form

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Check-in: /86 Check-out: /86  

Deposit: ¥20,000 × rooms = ¥

Note:  
- Application should be accompanied by the remittance of a hotel deposit of 20,000 yen per room.
- Room charges do not cover meals. A 10% tax and 10% service charge will be added at Sunshine Prince Hotel.
- No personal check is accepted. All payments should be in Japanese yen.

- Enclosed is a bank draft payable to JTB.
- Remitted on (date) through (name of your bank) to JTB at:

Bank of Tokyo, Marunouchi Branch,
Acct No.: 211694 (Ref. CD6-7401-86)

Please complete this form and send to: Secretariat - ISCA’86 Hotel Accommodation.