Multiprocessing refers to the simultaneous/concurrent execution of processes on independent nodes of a computer system. It has been presented in various forms in multiprocessor systems, multiple-processor systems, multicomputers, distributed computing systems, computer networks, and even vector processing systems.

For a number of years, simultaneous/concurrent processing has been implemented mainly in pipelined and array processors. People concluded that architectural concepts and the technology base that supported previous generations of computer systems had reached the end of their evolution.
Facing new challenges in strategic computing and intelligence processing and with requirements for very large-scale integrated circuit technology, researchers engaged in a multinational race to design and implement better computer systems. They seek innovative architectures that allow explicit, arbitrary multiprocessing and improve performance. The time for true multiprocessing has come. It is not the time for renovating an old idea, but for creating new perspectives for multiprocessing systems based on projected requirements and technology bases.

This special issue is aimed at marking the beginning of a new multiprocessing era. We are fortunate to be able to present six articles that give a perspective on the underlying multiprocessing technologies.

The first article by Gajski and Peir presents some essential issues in the design of multiprocessor systems; each of which employs two or more independent processing nodes under the control of a single operating system. The authors classify multiprocessing techniques according to methods of execution-sequencing and the degree of parallel execution of job, task, process, and instruction. According to sequencing methods, a multiprocessor system can provide data-driven, control-driven, or demand-driven executions. It can execute multiple tasks of a job, multiple processes of a task, or multiple instructions of a process simultaneously. In each of the multiprocessor categories, there are three basic problems: partitioning, scheduling, and synchronization. In addition, multiprocessing involves access to shared memory or distributed memory through interconnected networks; the authors survey techniques for shortening the memory access time.

In the second article, Patton explains multiprocessor architecture in terms of application orientations: throughput, availability, and response. Architectural innovation must respond to application requirements, and software development should follow the applications/architecture engagement. The author provides a contrast between supercomputing and fifth-generation parallel processing goals. An interesting sequence for future research is provided; the sequence starts with identification of intrinsically parallel applications and is followed by the development of parallel algorithms and definition of parallel computation models. Expressive parallel languages are then designed to map the application and algorithm onto the model in various granularities. Finally, architecture, support software, and hardware realization are implemented in sequence.

The third article by Schneck, Austin, Squires, Lehmann, Mizell, and Wallgren brings together descriptions of the major programs in parallel processing sponsored by the federal government. It samples the concerted design effort in computer systems to meet application needs and foreign competition.

In his article, Hwang surveys contemporary supercomputer systems, many of which have been introduced to private industry through federally funded projects. Huang places them in three architectural classes: pipelined computers, array processors, and multiprocessor systems. Pipelined multiprocessors represent the latest design in supercomputers. Many supercomputer manufacturers use this architecture to upgrade their high-end model. Except for some experimental systems, however, most multiprocessors are designed for data and information processing. Many computer professionals believe that application of the supercomputer should be extended to knowledge and intelligence processing.

Scientific computing and intelligence processing represent two main application domains of multiprocessing. The next two articles explore specialized domains. In Japan, the Institute for New Generation Computer Technology has been conducting research and development on fifth-generation computer systems since 1982. The major goal is to endow computers with knowledge and reasoning capabilities similar to those of humans. The article by Murakami, Kakuta, Onai, and Ito presents a new perspective on the fifth generation computer and describes operation principles of two core components, the parallel inference and knowledge base machines, which are to be prototyped and integrated into the system. The multinational competition looks extremely keen.

The article by Wah, Li, and Yu also deals with artificial intelligence, specifically with search problems that are unavoidable in intelligence processing. They investigate three paradigms of representations for combinatorial search problems. It is shown that functional requirements on architectures for search algorithms in each paradigm depend on algorithms, granularity, task scheduling, and synchronization. This study indicates that a versatile multiprocessing system reconfigured to meet changing functional requirements is crucial for AI applications.

Chuan-lin Wu has been on the faculty of Department of Electrical and Computer Engineering at the University of Texas at Austin since September 1, 1981. Wu has been teaching and publishing extensively on computer architecture, parallel processing, computer networks, and VLSI systems design. He also edited a special Computer issue devoted to interconnection networks (December 1981) and co-edited with T. Feng a tutorial on interconnection networks.

A senior member of IEEE, Wu has been a distinguished visitor of Computer Society since 1983. He has also been serving as an editor for IEEE Transactions on Computers and the Computer Society Press.

Questions about the general content of this special issue of Computer can be addressed to Wu, Dept. of Electrical and Computer Engineering, University of Texas, PO Box 7728, Austin, TX 78712.