Preliminary Program

NINTH ANNUAL INTERNATIONAL SYMPOSIUM ON COMPUTER ARCHITECTURE

April 26–29, 1982
Austin, Texas

Sponsored by
IEEE COMPUTER SOCIETY
acm ASSOCIATION FOR COMPUTING MACHINERY

MONDAY, APRIL 26
Tutorial
Algorithmic Computer-Aided Design for VLSI—T. Kehl

TUESDAY, APRIL 27

Session 1: High Level Languages
RISC Assessment: A High-Level Language Experiment—D. Patterson, R. Pieplo
Measures of Instruction Use by an Enhanced Instruction Computer—D.W. Clark, H.M. Levy
HLL Architectures: Pitfalls and Predictions—K. Kavi, B. Belkhoucha, E. Bullard, L. Delcambre, S. Nemecek

Session 2: Integrated Systems
VLSI Architectures for High-Speed Recognition of Context-Free Languages and Finite State Languages—K.H. Chu, K.S. Fu
Asynchronous and Clocked Control Structures for VLSI Based Interconnection Networks—M. Franklin, D. Wann

Session 3: Interconnection Networks I
Performance and Fault Tolerance Improvements in the Inverse Augmented Data Manipulator Network—R.J. McMillen, H.J. Siegel
The Gamma Network: An Interconnection Network for Multiprocessor Systems with Redundant Paths—D.S. Parker, C.S. Raghavendra
A Control Processor for a Reconfigurable Array Computer—R.M. Jenevein, J.C. Browne
A General Class of Processor Interconnection Strategies—L. Bhuyan, D.P. Agrawal

WEDNESDAY, APRIL 28

Session 4: Dataflow Architectures
A Dataflow Architecture with a Paged Memory System—L. Caluwaerts, J. Debacker, J.A. Peperstraete

Session 5: Design Approaches
Sentry: A Novel Hardware Implementation of Classic Operating System Mechanisms—G.C. Barton
A Logic Simulation Machine—M. Abramovici, Y.H. Levendel, P.R. Menon
Towards a Family of Languages for the Design and Implementation of Machine Architectures—S. Dasgupta, M. Olafsson

Session 6a: Fault Tolerant Computing
Design of a 2x2 Fault-Tolerant Switching Element—C. Wu, W. Lin
Fault-Tolerant Wafer-Scale Architectures for VLSI—D. Fussell, P. Varman

Session 6b: Database Systems
Database Filters—S. Pramanik
Hardware Sorter and its Application to Data Base Machine—Y. Dohi, et al.

Session 7a: Applicative Language Architectures
A Recursive Computer Architecture for VLSI—P.C. Treleaven, R.P. Hopkins
An HLL-RIS Processor for Parallel Execution of FP-Language Programs—M. Castan, E.I. Organick
The Heap/Substitution Concept—An Implementation of Functional Operations on Data Structures for a Reduction Machine—F. Hommes

Session 7b: Distributed Processing
A Shared Resource Algorithm for Distributed Simulation—P.F. Reynolds, Jr.
Duplication of Packets and their Detection in x.25 Communication Protocols—B.N. Jain
A Multiple Processor System for Real Time Control Tasks—P. Markenscoff

THURSDAY, APRIL 29

Session 8: Multicomputers
A Heterogeneous Multiprocessor Design and the Distributed Scheduling of its Task Group Workload—L.J. Miller
A Dual Processor Vax 11/780—G.H. Goble, M.H. Marsh
Effects of Cache Coherency in Multiprocessors—M. Dubois, F.A. Briggs

Session 9: Interconnection Networks II
Probabilistic Analysis of a Crossbar Switch—T.N. Mudge, B.A. Makrucki
Finding an Extremum in a Network—S.P. Levitan and C.C. Foster
Resource Allocation in Rectangular SW Banyans—U. Premkumar, J.C. Browne

***PLUS: panel sessions, plant trips, award luncheon, cocktail hours

For Complete Brochure and Registration Information
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