8 Array Processor Architecture: Guest Editor's Introduction

Douglas J. Theis

11 Architectural and Software Issues in the Design and Application of Peripheral Array Processors

Walter J. Karplus and Danny Cohen

How can we overcome the limits of von Neumann architecture and avoid supercomputer costs? This overview suggests that peripheral array processors are the answer in many applications.

18 An Approach to Scientific Array Processing: The Architectural Design of the AP-120B/FPS-164 Family

Alan E. Charlesworth

Architecture, not hardware, gives the FPS array processor family its computational speed. Here is an inside look at the trade-offs and ideas that went into its design.

28 Functionally Parallel Architecture for Array Processors

Edmund U. Cohler and James E. Storer

Based on the natural division of mathematical problems, functional parallelism becomes the architectural key for improving speed/cost ratios for array processors.

41 Integrating an Array Processor into a Scientific Computing System

Neil Maron and Thomas A. Brengle

When are array processors cost effective? How do they stack up against the supercomputers? This analysis weighs the many factors involved in answering these questions.

46 Precompilation of Fortran Programs to Facilitate Array Processing

Brian Brode

The automatic recognition of array operations in Fortran programs can now be applied to attached array processors using vectorizing precompiler software.

53 Array Processors: A Selected Bibliography

Thelma Louie

SPECIAL FEATURES

60 Structures for Advanced Information Systems

Edwin J. Smura

77 Tutorial Series—12: Design of a Small Business Data Processing System

Frank G. Soltis

95 The Open Channel:

Stopping the Arms Race Alan Hochberg

OAT: Testing to Minimize Undesirable Side Effects David A. Feinberg

Backing into Reliable Software Richard D. Ferrante

97 Compsac 81 Advance Program

130 IEEE Computer Society Officer and Governing Board Nominees

DEPARTMENTS

4 Letters to the Editor

105 New Products

116 IC Announcements

118 Microsystem Announcements

120 New Applications

125 Update

137 Short Courses

140 Call for Papers

144 Calendar

150 Classified Ads

151 Book Review: Principles of Database Systems

152 Advertisers/Product Index

153 The Bookshelf

Reader Service Cards, p. 152A; Order Form, p. 152C.

Computer Society Membership Application, p. 7.

IEEE Student Membership Application, p. 114.
September 1981

Use order form on p. 152C.

ISAAC NEWTON USED AN APPLE TO DISCOVER GRAVITY. WE ALSO USE AN APPLE® FOR VERY DOWN-TO-EARTH REASONS.

D²P. It’s EAI’s Digitally Directed Parallel Processor—a colorful new dimension in dynamic systems simulation and data acquisition. Lower costs, higher speeds, greater efficiency in solving dynamic simulation problems.

D²P combines the EAI 2000 parallel processor with the digital direction of an economical, well-supported microcomputer, and brilliant color CRT displays. It’s an exponential advance that includes dual floppy disc memory, EAI D²P software routines and the ability for you to program in PASCAL, FORTH, BASIC or ASSEMBLER.

It can handle up to 26 differential equations simultaneously, with up to 64KB of microcomputer main memory plus 250KB or more in mass storage...to use for either D²P or digital processing applications. Because D²P has parallel processing speeds up to 15 MOPS, it can clean up a lot of problems.

Contact Bill Kaplan at 800-631-4198 or, in New Jersey, at 201-229-1100 for details on how our D²P can help your discovery process.