advance program

VLSI

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FEBRUARY 23-26 spring compcon81

TWENTY-SECOND COMPUTER SOCIETY INTERNATIONAL CONFERENCE
JACK TAR HOTEL, SAN FRANCISCO, CALIFORNIA
TUTORIAL 1
Distributed System Design

Instructors: Michael P. Mariani and David F. Palmer

Audience: Intended for data processing systems engineers and designers. Also of interest to first and second level technical managers. Not intended for detailed hardware designers.

Course Description: We may approach the design of a distributed computing system with enthusiasm. The opportunity of molding custom architectures of hardware and software components to an enhanced throughput, reliability, "change-ability," etc., inspires our artful selves. The many options for exploiting parallelism, concurrency, redundancy, modularity, decentralized control, and data base distribution give a very rich design decision space. Unfortunately, the options also present overwhelming complexity, and design management can quickly become impossible as the project size increases.

This tutorial provides a procedure for treating design decisions in an orderly, viable manner. It describes techniques and computer aids applicable to specific steps of the procedure. Geographical, local system, and elemental component distributions are treated. Examples are drawn from stressing, real-time systems, and multicomputer testbed simulations.

Michael P. Mariani is program manager for TRW's Distributed Processing Architecture Design Program, which is directed at establishing the architecture technology necessary for low-risk design and development of stringent real-time, data-driven systems. Mariani is an IEEE Distinguished National Lecturer for 1979-1980 and a member of IFIP TC 10.3 Working Group on Digital Systems Design. He is a graduate of the University of Illinois.

David F. Palmer is manager of the Distributed Processing Requirements Engineering Program, General Research Corporation, where he has been developing requirements for software/hardware tradeoff decisions leading to customized, distributed architectures. He has taught courses in electrical engineering and computer science at the University of California, and is an IEEE Computer Society Distinguished National Lecturer for 1979-80. Palmer holds a PhD in electrical engineering from Duke University.

Course Outline:
Distributed System Design Rationale

Analysis Steps: identification • elaboration • operational requirements accommodation • verification
Partitioning Steps: criteria selection • relationship evaluation • thresholding
Allocation Steps: architecture dimensionality determination • module mapping • resource requirements update • performance-cost-reliability analysis
Synthesis Steps: interconnect architecture design • high fidelity performance analysis • pay-off models • analytic contention models • discrete event simulations

Summary and Conclusions

TUTORIAL 2
Local Computer Networks

Instructor: Harvey A. Freeman

Audience: Intended for managers, engineers, system analysts, designers, and students. Some experience in computing and some exposure to data communications would be helpful.

Course Description: This introductory level tutorial addresses local computer networks, a class of systems which are generally owned by a single organization, cover distances on the order of a few miles, and use a communication sub-network technology such as packet switching, circuit switching, or busing. First, the overall definition and context of LCNs are described. Then important design issues and potential solutions currently identified for LCNs are discussed. This is followed by a number of case studies of important local computer networks. LCNs which evolved from distributed processing contexts and those which evolved from attempts to upgrade and enhance current large-scale systems are covered. Conclusions provide a view of the future directions of LCNs.

Harvey A. Freeman is manager of the Data Systems Design Department at Sperry Univac. He currently manages an advanced development group investigating and developing concepts, techniques, and specifications for large-scale Sperry Univac computer systems in distributed processing environments, including local, backbone, and non-homogeneous networks. He is a co-author of the book, Data Base Computers. Freeman is also an adjunct professor in the computer science department at the University of Minnesota. He holds a PhD in electrical engineering from the University of Illinois.

Course Outline:
Background: definition • evolution • taxonomy • examples
Design Issues: network entities • network architectures • network operation • performance • user considerations
Case Studies: HYPERchannel • ETHERNET • Cambridge Ring • selected others
Future Directions: gateways • commercial availability • trends

Conclusions

TUTORIAL 3
Computer-Assisted Design and Engineering

Instructors: Stephen R. Levine and Bruce Eric Brown

Audience: Managers, users, and persons responsible for specifying computer-assisted design and engineering systems. Professionals who will use these systems need no background in computer science.

Course Description: This introduction to the use of computers and computer graphics in design and engineering describes the hardware and software of current and future systems. Other topics covered include system requirements, cost trade-offs, system integration, facility management, and user training. Expectations for the near future will be presented.

Stephen R. Levine is president of Electronic Graphics Associates, a firm specializing in computer graphics consulting and systems integration. He also teaches an international short course on computer graphics, and has consulted widely on the subject. His previous experience includes eight years with Lawrence Livermore National Laboratory, where he directed the development of new computer graphics hardware and software, including the joint development of the Dicom D148 color film recorder, three years with Stanford Research Institute, and two years with Singer Simulation Products. Levine is a past president of the National Computer Graphics Association, a current director and a former vice chairman and treasurer of ACM's SIGGRAPH. He received a BS and an MS in electrical engineering from the University of California, Berkeley, and a PhD in computer science from Stanford in 1975.

Bruce Eric Brown is a mechanical engineer at Lawrence Livermore National Laboratory, where he is responsible for engineering computer graphics and the integration of a CAD system to an analytical modeling system. He is also actively engaged as a consultant. Active in computer graphics since 1969, he has published several papers on the applications of computer graphics to civil and mechanical engineering problems. Before joining Livermore Lab, he worked at the Los Alamos Scientific Laboratory and for the Navy as a research structural engineer. A graduate of Brigham Young University, he received the BS and MS in civil engineering in 1974; he received the PhD in computer science from the University of Utah in 1977.

Course Outline:
Introduction: hardware • software • state-of-the-art
Applications: present • future • assessing needs
Systems: specification • evaluation • cost trade-offs • utilization • training • managing
Future: near term expectations
TUESDAY, February 24, 1981

9:00am–noon
OPENING CEREMONY
KEYNOTE ADDRESS: “The Next Revolution in Electronics” — Carver Mead

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<td>SESSION 2: VLSI Forecasting</td>
<td>SESSION 3: Mini Winchester Disks</td>
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<td>Chairperson: Skip Stritter</td>
<td>Jim Rudolph</td>
<td>Stephen Marcy</td>
<td>SESSION 4: Impact of Software on Microprocessor Architecture</td>
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<td>SESSION 6: Packaging Can Limit the Use of VLSI</td>
<td>SESSION 7: Applications for VLSI</td>
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<td>Chairperson: Maris Graube</td>
<td>Rex Rice</td>
<td>R. Mueller</td>
<td>SESSION 8: Non-Traditional Research Issues in Computer Engineering</td>
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5:00pm
COCKTAIL HOUR

WEDNESDAY, February 25, 1981

8:30–10:00am
SESSION 9: Data Base Machine Architecture
Jim Goodman

SESSION 10: Semiconductor Memories
James Early

SESSION 11: VLSI in Speech Processing
Bruce Lowerre

SESSION 12: Ada: Fear and Loathing in Programming
Dennis Allison

10:30am–noon
SESSION 13: Data Flow Architectures
Sam Gebala

SESSION 14: Gate Arrays and Programmable Logic
Tom Goodman

SESSION 15: Recent LSI Implementations of Multiple-Valued Logic
David Rine

SESSION 16: Operating System Topics
Dennis Allison

1:30–3:00pm
SESSION 17: Attached Array Processors
Phil Kuekes

SESSION 18: The New CMOS Microprocessor Era Is Dawning
Bill Huston

SESSION 19: Intelligent Data Entry
William R. Smith

SESSION 20: Migrating UNIX to Micros
Bob Marsh

3:30–5:00pm
SPECIAL ADDRESS:
“Prometheus or Pandora: The Influence of Automation on Society” — Herbert A. Simon

5:00pm
COCKTAIL HOUR

THURSDAY, February 26, 1981

8:30–10:00am
SESSION 21: Multiprocessor Systems Architecture
Steve Ward

SESSION 22: VLSI Testing
Edward J. McCluskey

SESSION 23: High Resolution Displays
Pat Mantey

SESSION 24: Disposable Intelligence: Hand-Held Computers
Paul Heckle

10:30am–noon
SESSION 25: Memory Management
Ted Lallioitis

SESSION 26: Technology Development of VLSI
H. J. Harloff

SESSION 27: Computerized Phototypesetting
Jonathan Sachs

SESSION 28: Software Mass Marketing
Jim C. Warren, Jr.

1:30–3:00pm
SESSION 29: 32-Bit VLSI Computers, Part I
Dave Patterson

SESSION 30: Computer-Aided Design Philosophy
Edwin Porter

SESSION 31: Intelligent Instrumentation
Chuck House

SESSION 32: Legal Views: Software Ownership, Value and Liability
David Harrison

3:30–5:00pm
SESSION 33: 32-Bit VLSI Computers, Part II
Dave Patterson

SESSION 34: Fiber Optic Communications Systems
Masao Kawashima

SESSION 35: Optical Data Disks
Steve Miller

SESSION 36: Public Information Utilities
Jim C. Warren, Jr.

5:00pm
END OF CONFERENCE
TUESDAY, February 24, 1981

9:00am OPENING CEREMONY

KEYNOTE ADDRESS: THE NEXT REVOLUTION IN ELECTRONICS
Carver Mead, Cal Tech

Historically, integrated circuit technology has been viewed as a mechanism for producing existing functions for lower cost. Today we MUST view VLSI in a new light: as a truly revolutionary medium for system design. Architectures capable of many orders-of-magnitude higher computational power than the largest existing mainframes will be possible with VLSI technology. These VLSI-based designs will be organized in a completely different way than current computing machinery. The key difference is that an enormous number of operations will be done concurrently, instead of sequentially as in today's machines. It is just starting to become clear what the outline of such radical architectures should be, and how they can be put to effective use. It is likely that the opportunities and challenges raised by this remarkable combination of VLSI technology and the intellectual framework for its use will cause major changes in the structure of the electronics industry.

Afternoon 1:30–3:00pm

SESSION 1: LOCAL NETWORKS
Chairperson: E. Stritter, Nestar Systems
LOCAL NETWORKS OF PERSONAL COMPUTERS — S. Stritter: Nestar Systems
ARCHITECTURE OF Z-NET, A MICROPICPROCESSOR-BASED LOCAL NETWORK — J. Estrin: Zilog
PERFORMANCE OF ETHERNET, A CONTENTION-BASED NETWORK — R. Yarar: Intel
LOCAL NETWORK DESIGN USING FIBER OPTICS — D. Sensig and R. Neff: Hewlett-Packard
LOCALNET: A DIGITAL COMMUNICATIONS NETWORK FOR BROADBAND CABLE — K. Biba: SYTEK

SESSION 2: VLSI FORECASTING
Chairperson: J. Rudolph, Gnostic Concepts
Panelists: H. Bogert, Dataquest; L. Lopp, Consultant; J. M. Connell, Tektronix

SESSION 3: MINI WINCHESTER DISKS
Chairperson: S. Marcy, Pertec
Speakers: D. Goodrich, Intel; E. M. Dunstan, Micropolis; R. Brooke, Pertec

SESSION 4: IMPACT OF SOFTWARE ON MICROPROCESSOR ARCHITECTURE
Chairperson: D. Conn, Fairchild
FINDING ARCHITECTURAL COMMONALITY BETWEEN SOFTWARE AND HARDWARE — L. W. Hoewel: IBM
MICROPROCESSOR ARCHITECTURE WHICH REFLECTS SOFTWARE REQUIREMENTS — H. C. Cragon: Texas Instruments
SOFTWARE IMPACT ON MICROPROCESSOR ARCHITECTURE: A CASE STUDY — R. Markowitz: Intel
COMPUTER ARCHITECTURE IN LSI: LESSONS AND PROSPECTS — D. G. Weiss: Motorola

Afternoon 3:30–5:00pm

SESSION 5: LOCAL NETWORK STANDARDS
Chairperson: M. Graube, Tektronix
IEEE 802 LOCAL NETWORKS — G. Clancy: Honeywell
OPEN SYSTEMS INTERCONNECTION MODEL — R. Shatz: Hewlett-Packard
ANSI 50-M BIT BUS — G. Milligan: Magnetic Peripherals
PROWAY PROCESS CONTROL NETWORK — W. Gellie: National Research Council of Canada

SESSION 6: PACKAGING CAN LIMIT THE USE OF VLSI
Chairperson: R. Rice, R² Consulting
VLSI PACKAGING ENVIRONMENT — R. Rice: R² Consulting
SYSTEM PACKAGING ECONOMICS OF VLSI — F. K. Buelow: STC
VLSI PACKAGING DESIGN CONSIDERATIONS — J. Nelson: Burroughs

SESSION 7: APPLICATIONS FOR VLSI
Chairperson: R. Mueller, Siemens Corp.
Speakers from Western Europe

SESSION 8: NON-TRADITIONAL RESEARCH ISSUES IN COMPUTER ENGINEERING
Chairperson: B. Chern, NSF
Panelists: A. Despain, University of California, Berkeley; H. Stone, University of Massachusetts; E. Davidson, University of Illinois; R. Reddy, Carnegie-Mellon University

WEDNESDAY, February 25, 1981

Morning 8:30–10:00am

SESSION 9: DATA-BASE MACHINE ARCHITECTURE
Chairperson: J. Goodman, University of Wisconsin
IS THERE AN IDEAL DATA BASE MACHINE — P. B. Hawthorne: University of California, Berkeley
UTILIZING ASSOCIATIVE ARRAY MEMORIES IN THE DESIGN OF A DATA-BASE COMPUTER — E. Oliver: Bell Laboratories

SESSION 10: SEMICONDUCTOR MEMORIES
Chairperson: J. Early, Fairchild
LARGE ECL BIPOLAR RAMs — J. Stinehelfer, R. Rufford, V. Catter: Fairchild
HIGH-SPEED NMOS 16K STATIC RAM — J. O'Toole: Mostek
64K DYNAMIC RAM — J. Chan, J. D. Barnes, D. A. Maxwell, J. Muschinske: Fairchild
NEW APPLICATIONS WITH E² PROMs — J. Rizzo: Intel

SESSION 11: VLSI IN SPEECH PROCESSING
Chairperson: B. Lowerre, Hewlett-Packard
APPLICATION OF LSI TO SPEECH RECOGNITION — B. Warren: AURICLE, Inc.
APPLICATION OF LSI TO SPEECH SYNTHESIS — R. Wiggins: Texas Instruments
AN INTEGRATED FRONT-END FOR DISCRETE WORD RECOGNITION — S. Viglione: Interstate Electronics
REMOVING "GAMESManship" FROM PERFORMANCE SPECIFICATIONS OF DISCRETE WORD RECOGNITION — B. T. Lowerre: Hewlett-Packard

SESSION 12: ADA: FEAR AND LOATHING IN PROGRAMMING
Chairperson: D. Allison, Stanford University
Panelists: To Be Announced

Morning 10:30am–noon

SESSION 13: DATA FLOW ARCHITECTURES
Chairperson: S. Gebala, Hewlett-Packard
A GRAPHICAL APPROACH TO SOFTWARE DEVELOPMENT USING FUNCTION GRAPHS — R. M. Keller and J. Yen: University of Utah
A FILE-ORIENTED APPLICATION PROGRAM FOR A DATA-DRIVEN COMPUTER SYSTEM — A. L. Davis and S. A. Lowder: University of Utah
AN INSTRUCTION SET FOR THE PROCESSING ELEMENT OF A MULTIPLE PROCESSOR DATAFLOW MACHINE — Arvind: MIT

SESSION 14: GATE ARRAYS AND PROGRAMMABLE LOGIC
Chairperson: T. Goodman, Fairchild
GATE ARRAYS: A USER PERSPECTIVE — T. Chaus: CDC
THE IMPACT OF CUSTOMIZED GATE ARRAY FAMILIES ON CUSTOM DESIGN — W. K. Owens: Fairchild
THE MASK-AND-FIELD PROGRAMMABLE LOGIC DESIGN REVOLUTION — G. A. Davis: Signetics
THURSDAY, February 26, 1981

Morning 8:30-10:00am

SESSION 21: MULTIPROCESSOR SYSTEMS ARCHITECTURE
Chairperson: S. Ward, MIT
MPC: A MULTIPROCESSOR/MULTICOMPUTER ARCHITECTURE — B. W. Arden and R. Ginosar, Princeton University
A VLSI INTERCONNECTION NETWORK FOR MULTIPROCESSOR SYSTEMS — C. Wu and T. Feng, Ohio State University
ARCHITECTURE OF A MYRIAPROCESSOR — R. Halstead: MIT

SESSION 22: VLSI TESTING
Chairperson: E. J. McCluskey, Stanford University
PRACTICAL MICROPROCESSOR TESTING: OPEN- AND CLOSED-LOOP APPROACHES — J. A. Abraham: University of Illinois
K. P. Parker: Hewlett-Packard
A CIRCUIT FOR DETECTING AND ANALYZING TEMPORARY FAILURES — E. J. McCluskey and J. F. Wakerly: Stanford University
SELF-TESTING BIT-SLICED MICROCOMPUTERS — T. Sridhar and J. P. Hayes: USC

SESSION 23: HIGH RESOLUTION DISPLAYS
Chairperson: P. Mantay, IBM
DISTRIBUTED SYSTEM DESIGN DISCIPLINE: AN APPLICATION OF TELL — J. H. Rhine and R. G. Dalpezzo: IBM
COMPUTER GRAPHICS: HARDWARE AND TECHNOLOGY DIRECTIONS — C. T. Masters: DeAnza Systems
THE GDS-2 SYSTEM FOR PHYSICAL DESIGN — T. Schafer: Calma Co.

Morning 10:30am-noon

SESSION 24: DISPOSABLE INTELLIGENCE: HAND-HELD COMPUTERS
Chairperson: P. Heckle, Interactive Systems Consultant
Panelists: G. Leiveille, IBM; M. Morand, IBM; G. Goldberg, Xerox PARC; D. E. Morris, Hewlett-Packard; E. Julisson, Texas Instruments

SESSION 25: MEMORY MANAGEMENT
Chairperson: T. Laliotis, Hewlett-Packard
FOURIER ANALYSIS OF SOFTWARE-CACHE INTERACTIONS — L. Hoovel: IBM
VIRTUAL MEMORY MANAGEMENT FOR THE 29000 — D. Stevenson: Zilog
DESIGN PHILOSOPHY OF THE 68000 MMU — J. Zolnowsky: Motorola
ADDRESS TRANSLATION AND MAPPING REDUCE RAM SIZE REQUIREMENTS — T. Laliotis: Hewlett-Packard

SESSION 26: TECHNOLOGICAL DEVELOPMENT OF VLSI
Chairperson: H. J. Harloff
Speakers from Western Europe

SESSION 27: COMPUTERIZED PHOTOGRAPHY SETTING
Chairperson: J. Sachs, Orthocode
TEX ON SMALL MACHINES — K. S. Harris and R. M. McClure: Unidot, Inc.
MANAGING TEXT OR TEXTUAL DATABASES — B. Bates: Link NEWSPAPER PUBLISHING SYSTEM — TODAY OR TOMORROW — P. Brainard: ARTEX

SESSION 28: SOFTWARE MASS MARKETING
Chairperson: J. C. Warren, Jr., Wireless Digital, Inc.
Panelists: B. Gates and V. Raburn, Microsoft; G. Kildall, Digital Research; D. Fylstra and T. Opendedyke, Personal Software; J. C. Warren, Jr., Wireless Digital, Inc.
**Afternoon 1:30–3:00pm**

**SESSION 29: 32-BIT VLSI COMPUTERS, PART I**
Chairperson: D. Patterson, University of California, Berkeley

AN EXTENSIBLE OPERATING SYSTEM FOR THE INTEL 432 — K. Kahn and S. Pollack: Intel


**SESSION 30: COMPUTER-AIDED DESIGN PHILOSOPHY**
Chairperson: E. Porter, STC

DIGITAL SYSTEMS AS MATHEMATICAL EXPRESSIONS — R. E. Frankel and S. W. Smolinar: General Research Corp.

PRIM: A PLACEMENT AND ROUTING IMPLEMENTATION SYSTEM FOR MASTER-SLICE LSI CHIP DESIGN — M. H. Young: STC

CAD FOR SIGNAL PROCESSING — S. Wharton: Intel

**SESSION 31: INTELLIGENT INSTRUMENTATION**
Chairperson: C. House, Hewlett-Packard

HP 1980 INTELLIGENT SCOPE — F. Rampey: Hewlett-Packard

NETWORK ANALYZER FOR B-767 — S. Kubota and W. Fagg: Interface Technology

COMPUTERIZED BLOOD ANALYSIS — I. Lee: Chemetrics

ARBITRARY WAVEFORM GENERATOR — W. Farnbach: Wavetek


**SESSION 32: LEGAL VIEWS: SOFTWARE OWNERSHIP, VALUE AND LIABILITY**
Chairperson: D. Harrison, Owen, Wickersham & Erickson

Panelists: D. Harrison and R. Carney, Owen, Wickersham & Erickson; others to be announced

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**Afternoon 3:30–5:00pm**

**SESSION 33: 32-BIT VLSI COMPUTERS, PART II**
Chairperson: D. Patterson, University of California, Berkeley

ARCHITECTURE OF THE NS 1600 SUPPORT HIGH-LEVEL LANGUAGES, OPERATING SYSTEMS — L. Cohn: National Semiconductor

Panelists: J. Rattner, Intel; L. Cohn, National Semiconductor; A. Despain, University of California, Berkeley

**SESSION 34: FIBER OPTIC COMMUNICATIONS SYSTEMS**
Chairperson: M. Kawashima, Fujitsu Labs

OPTICAL FIBER MAKES RESEARCH INFORMATION PROCESSING SYSTEM — K. Yada: Electro-Technical Lab; T. Ochiai and M. Honda: Fujitsu Labs

MINICOMPUTER SYSTEM DISTRIBUTION BY OPTICAL FIBER DATA HIGHWAY — K. Yamaguchi, Y. Suzuki, R. Yatsubachi: Fujitsu Labs

OPTIC FIBER DATA FREEWAY SYSTEMS — A LOOP NETWORK FOR DISTRIBUTED COMPUTER CONTROL — M. Yanaka: Hitachi

IMPACT OF TERMINAL DEVICE DESIGN ON FIBER OPTIC LOCAL AREA NETWORKS — D. Hanson: Hewlett-Packard

**SESSION 35: OPTICAL DATA DISKS**
Chairperson: S. Miller, SRI

OPTICAL DATA DISK TECHNOLOGY — L. J. Laub: Exxon Enterprises, Inc.

I/O SUBSYSTEM DESIGN — T. D. Dodd: STC

**SESSION 36: PUBLIC INFORMATION UTILITIES**
Chairperson: J. C. Warren, Jr., Wireless Digital, Inc.

Panelists: J. C. Warren, Jr., Wireless Digital, Inc.; R. Larratt, Infomart; R. Plummer, Institute for the Future

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<td>Tutorial 1 — Distributed System Design</td>
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<td>Tutorial 3 — Computer-Assisted Design and Engineering</td>
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NOTE:
Requests for refunds must be received in writing no later than February 13, 1981. Tutorial registration fee must be received in writing by February 13 to insure enrollment. Conference registration fee includes one copy of the COMPCON Digest of Papers, as well as two (2) complimentary drink tickets for each of the conference-hosted parties, Tuesday and Wednesday nights.

Late registration will be accepted at the Jack Tar Hotel beginning Sunday evening, February 22, 1981. The fee for late registration is an additional $10 for the conference or tutorial or an additional $20 if both are selected.

Complete and mail this reservation form to:
Jack Tar Hotel, Van Ness at Geary, San Francisco, CA 94101, Telephone (415) 776-8200

Reservations must be received by the Jack Tar Hotel prior to January 24, 1981. Rooms will be held until 6 p.m. on day of arrival unless accompanied by deposit to cover first night's lodging. A block of rooms has been set aside for COMPCON. If calling, be sure to mention that you are attending COMPCON.

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