The 1980 International Symposium on Fault-Tolerant Computing — 10th in a series of international meetings devoted to the theory and practice of reliable computing

PRELIMINARY PROGRAM

OCTOBER 1 — Wednesday Morning

Opening Remarks — 10:00 a.m.
Steering Chairperson — Hisashi Mine (Kyoto Univ., Japan)
Program Chairperson — Yoshihiro Tomita (Tokyo Inst. of Tech., Japan)

1A — Commercial Systems — 10:40–12:00

1B — Design Verification — 10:40–12:00

OCTOBER 1 — Wednesday Afternoon

2A — Coding for Mass Storage — 13:30–14:50
3. “Random-Double-Track-Error Correction in Magnetic Tapes,” A. K. Bhattacharya, Sperry Univac, USA; L. L. Kniesy, Univ. of Minnesota, USA.

2B — Operating Systems and Synchronization — 13:30–14:50

3A — Correction of Memory Faults — 15:10–17:10
3. “A Design for Process State Preservation after Storage Unit Failure,” J. A. Arulpragasam and R. S. Swartz, DEC, USA.
4. “Masking Triple Fixed Defects in Memory,” Roznetsof Academy of Sciences, USSR

3B — Software Fault Avoidance and Tolerance — 15:10–17:10
4. “Application of Fault-Tolerant Deadline Mechanisms to a Satellite On-Board Computer System,” A. Y. Wei, K. Hirasawa, R. Cheng, and R. R. Campbell, Univ. of Illinois, USA.

Reception — 17:30–19:00

OCTOBER 2 — Thursday Morning

4A — LSI Testing: 1 — 9:30–10:40

4B — Modelling for Evaluation: I — 9:30–10:40
1. “Performance-Reliability Model for Computing Systems,” A. Castiello and D. P. Sierk, CMU, USA.

5A — LSI Testing: II — 11:00–12:00
1. “FPTLA: A Programmable Array Logic Array For Function Independent Testing,” S. J. Hong and D. L. Ostapko, IBM, T. J. Watson Research Center, USA.

5B — Modelling for Evaluation: II — 11:00–12:00

OCTOBER 2 — Thursday Afternoon

6A — Test Generation: 13:30–15:10
1. “An Implicit Enumeration Algorithm to Generate Test for Combinational Logic Circuits,” P. God, IBM Data Systems Division, USA.

6B —Coverage Evaluation — 13:30–15:10
2. “Robust Detection of Intermittent Faults,” J. S. Stiller, Raytheon, USA.


7B — Evaluation as a Design Aid — 15:30–17:30

Banquet — 19:00–21:00
OCTOBER 3 — Friday Morning

8A — Self-Checking: I — 9:00-10:20

8B — Distributed System Architectures — 10:40-12:10
1. "A Highly Reliable Distributed Loop Network Architecture," A. Gmarov, L. Kleinrock, and M. Gerla, UCLA, USA.

9A — Self-Checking: II — 10:40-12:10

9B — Fault-Tolerant Logic Design — 10:40-12:00

OCTOBER 3 — Friday Afternoon

10A — System Level Diagnosis — 13:30-14:40

10B — Dedicated Systems — 13:30-15:30

11 — Multiple Fault Test Generation — 14:50-15:40
2. "Fault Diagnosis in Sequential Circuits Based on an Effect-Categories," M. Abramowitl and M. A. Breuer, USA.

For Information Contact:
Professor John F. Meyer
Vice Chairperson, FTCS-10
Department of EE and CE
The University of Michigan
Ann Arbor, MI 48109
Telephone: (313) 763-0037

For Special Travel Arrangements Contact:
Garber Travel
1406 Beacon Street
Brookline, MA 02146
(617) 556-2100

ACCOMMODATION APPLICATION FORM
10th International Symposium on Fault-Tolerant Computing
Please complete (type or print in block letters) and return this form by August 30, 1980.

Title (circle one): Prof. / Dr. / Mr. / Mrs. / Miss / Ms.
Name: ____________________________
Mailing Address: ____________________________
Telephone: ____________________________

Your Arrival Schedule:
(date) (airport) (flight)

Accompanying Name (if any):
I (We) need the following hotel accommodations:
(Fill in the boxes with numerals or check marks.)

<table>
<thead>
<tr>
<th>Hotel Name</th>
<th>Twin</th>
<th>Single</th>
<th>Period of Stay</th>
</tr>
</thead>
<tbody>
<tr>
<td>Kyoto Hotel</td>
<td>☐ Y12,800</td>
<td>☐ Y7,940</td>
<td>Check in:</td>
</tr>
<tr>
<td>A class room</td>
<td>☐ room</td>
<td>☐ room</td>
<td></td>
</tr>
<tr>
<td>B class room</td>
<td>☐ Y9,800</td>
<td>☐ Y6,640</td>
<td>Check out:</td>
</tr>
</tbody>
</table>

Travellers Inn ☐ Y7,000 ☐ Y5,800

Travelers Inn ☐ Y7,000 ☐ Y5,800

The above room rates include 10% tax and 10% service charge, but no meals.
I (We) need the following other travel arrangements:

Date: __________ Signature: __________

Japan Travel Bureau, Inc. (JTB) will send you the confirmation letter.

IT'S LESS EXPENSIVE THAN YOU MIGHT THINK!
- LOW Conference Hotel Rates: $17 (beginning rate: single room/bath)
- LOW Air Fares: $715 (APEX High Season Fare: round trip LA/Tokyo)
- ANOTHER REASON for going: IFIP '80 will be held the following week in Tokyo — October 6-9