A record 930 attendees met February 27-March 1 in San Francisco, where they explored the conference theme of "Exploding Technology, Responsible Growth."

**WRAP-UP**

**The Barriers to Technology**

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*Computer staff*

In 1959 Robert Noyce invented the silicon monolithic integrated circuit. A few years later Gordon Moore decreed that the number of elements contained on a chip would double each year, with the more potent chips costing approximately the same amount year after year. These two events, according to John G. Linvill of Stanford University, marked the inception of a technology that has since exploded spectacularly.¹

Linvill was one of a panel of four plenary session speakers at COMPCON 79 Spring in San Francisco February 27. Other speakers at the opening session included consultant Robert M. McClure, William Miller of Stanford University, Arnold Mitchell of SRI International, Myron Tribus of MIT, and consultant Cuthbert Hurd (who chaired the session).

Moore’s law has fairly accurately predicted the course of the explosion for almost two decades and promises to maintain its predictive accuracy to the mid 1980s. Referring to a recent point on the curve, Linvill cited the production of a 64K-bit CCD bulk memory incorporating 135,000 elements on one chip.

Solid state disk. The CCD chip, which has been employed in a storage subsystem by Storage Technology Corporation,² is a dynamic MOS memory device organized as sixteen 4096-bit serial shift registers (loops). The data in the loops circulates continuously at a clock rate of 1 to 3 MHz. At the latter frequency the average access time is approximately 0.7 millisecond.

The chips are organized into a 72 x 24 matrix, providing a word length of 8 bytes plus one error-detection-and-correction byte. Array capacity is 12 megabytes.

With a control unit the storage array emulates the IBM 2305-2 fixed-head disk, attaching to IBM 370 (135 and larger) and 303x CPUs via the block multiplexer channel. It operates with OS, VS1, VM, and MVS operating systems. A fully configured solid state disk (four storage arrays) is equivalent to two 2305-2 facilities. However, STC says that the average access time is about one seventh that of the magnetic disk.

General Chairman Dean Brown of Picodyne welcomed attendees and five speakers to the keynote session. Brown noted the computer profession’s growing concern with the human implications of computer technology.

Program Chairman Fred Buelow of Microtechnology Corporation introduced the conference’s 25 technical sessions. Topics ranged from hardware (e.g., VLSI design) to software and applications (e.g., voice systems and computer graphics).
addition, it is less costly, consumes less power, and requires less floor space. Perhaps this disk replacement will prove to be the product that will establish CCDs in the market place. The promise of 256K chips in 1980 should confirm CCD’s cost effectiveness.

Addressing the same subject in Session 6, “Architecture and Technology for Data Management,” G. A. Champine of Sperry Univac concludes that CCD’s historical lead of 18 to 24 months over RAM makes them “attractive in high speed swapping stores and disk caches for large mainframes.” On the other hand, Itel Vice-President John Bock opined in Session 23, a panel discussion of plug-compatible computers, that “CCDs have pretty much missed their window,” referring to the “moving target” that magnetic recording technology presents. In the same vein, Al Hoagland of IBM, speaking in Session 6, expects the moving-head-disk technology to maintain its relative cost advantage per bit over CCD—as well as magnetic bubbles—at least through 1985.

Magnetic bubbles. This gap-filler technology now seems to be regarded a bit more favorably than CCDs.Quarter-million bit chips were announced last year by Rockwell International and Texas Instruments. One-megabit units may be available in 1980 or 1981. Both Champine and Hoagland forecast their use in small systems, the latter saying, “Magnetic bubble memory should fare better [than CCDs] against the floppy disk in small systems where total cost (i.e., capacity) rather than cost per bit is the key factor.”

(A glimpse of the somewhat more distant future was provided by Y. S. Lin and his colleagues of the IBM Thomas J. Watson Research Laboratories a couple of weeks after COMP- CON Spring at the International Colloquium on Magnetic Bubbles. The IBM group has fabricated a 2000-bit test chip using a contiguous-disk pattern that packs smaller bubbles in a 16-times denser structure, but still uses current optical lithographic resolution. Chips containing several megabits of storage would be possible if the research proves transferable to production.)

Magnetic disks. Magnetic recording served the computer 30 years ago when the CPUs still used vacuum tubes. Obviously, by now it is a “mature” technology. Less obviously, it still belongs under the exploding technology rubric. For example, according to Champine “Capacity of a state-of-the-art moving-head disk increased from 25 megabytes in 1969 to 350 MB in 1978 and is projected to reach 700 MB in 1980 and 1000 MB in 1982. Density increased from 300 bits/cm² in the early 1960s to 500,000 bits/cm² currently. The historical cost-reduction rate of a factor of two every 30 months should continue for at least several more years. Thin film heads offer lower cost and higher performance.”

Main memory. The effect of advancing silicon technology on memory density and cost per bit is now well known. However, as Champine phrases it, “the general pattern has been to quadruple the number of bits on a chip every three years; this has cut the price approximately in half every three years.”

Illustrating this rule with a system-level comparison, Soltis and Hoffman (Session 12, “Small Business Systems”) compared two IBM computers 10 years apart. The price of an additional 16 KB of 1500 nano second/byte main storage for the IBM System/3 5410 (Model 10) processor was over $20,000 at the time of announcement in 1969. Today the System/38 5381 Model 3 offers an additional 256 KB of 1100 ns/4 bytes main storage for $5000. In this comparison cost per byte has dropped more than 64-fold and performance has improved over five times in less than 10 years.

If the rule continues to be valid, 64K chips should be in production in 1980, 256K samples should be offered in 1982, and a 1-megabit chip should appear later in the same decade.
Less often noted has been the effect of more economical RAM in shifting the system balance toward main memory. This effect has increased processor utilization "from the 50 to 60 percent common in the early 1970s to the 85 to 95 percent common today." More main store has also reduced the time spent in operations. Thus, dropping memory costs have contributed substantially to CPU performance.

Processor performance. "The performance of large-scale computers has improved by a factor of four every 5 years," reports William C. Chow of Amdahl Corporation. "This trend will continue in the next decade." He attributes it to large-scale integration.

Similarly, at the other end of the processor scale, circuit densities of up to 70,000 transistors per chip are resulting in microprocessors with the capabilities of minicomputers. Moreover, the number of elements now attained on one chip is only an order of magnitude from the number in large-scale computers.

Certifying to the strength of the new technology, more than a dozen companies are now producing 16-bit microprocessors. The Intel 8086, Motorola MC68000, and Zilog Z8000 have been described at length in recent issues of this magazine. Stritter and Gunter, in particular, make the point that the MC68000 is only the initial version of a number of eventual implementations. This first chip embodies only the subset permitted by current technology of the ultimate architecture. The total architecture has already been planned to encompass additional features that expected advances in technology will make possible.

New 16-bit processor. Nippon Electric Company's μCOM-1600 may function as either a master or slave microprocessor, depending on the level applied to its mode input. Two of the units, when connected to dual buses, comprise a multimicroprocessor system.

Each processor is connected to its own local units, such as ROM, RAM, or I/O controllers by means of a so-called internal bus. Units to be used by both processors, such as main memory and peripherals, are attached to a common bus.

The master processor arbitrates use of the common bus. In response to requests from DMA units or the slave processor, the master processor authorizes the requesting unit to use the common bus. It accomplishes this by electrically disengaging itself from the bus. While the common bus is occupied, e.g., by a DMA operation between main memory and a peripheral, the master processor may continue to execute instructions from its local ROM, at least until some instruction necessitates a main memory access. Thus, processor efficiency is enhanced by enabling a processor to continue local operations while the common bus is in use.

Barriers to exponential growth

Like other industry observers, Linvill forecasts the attainment of hundreds of thousands of elements on a single chip sometime in the 1980s. However, he identified some "potent barriers" to continuing the past rate of exponential growth:

Physical barriers. To attain high speed (VHSI) and high density (VLSI), the device designer strives to make the chip structure small. Line widths are already reaching the limit of optical resolution and further density will require the resolution attainable by electron-beam lithography, which was the subject of one of the three COMPCON tutorials. Further out is x-ray lithography.

As structures become smaller, ion implantation promises to provide the fine distribution of impurities needed. But the process of implanting ions creates surface damage and annealing it out by conventional thermal methods diffuses the impurity distribution. What is needed is an annealing technique as dimensionally precise as the structures themselves. Linvill suggests the use of a laser or electron beam for this task.

With the movement to smaller linear dimensions, the ratio of surface area to volume is changing. The need to analyze the emerging surface and interface phenomena is calling the solid-state physicist back to center stage.

On-chip connections. At fine dimensions still another phenomenon requires consideration: the polycrystalline connections between elements become little RC transmission lines with growing transit times. In fact, stated Linvill, the limiting factor is no longer the switching element but the signal path.

On-chip interconnect delays, however, are only one consideration for the system designer concerned with maximizing processing speed. As analyzed by A. A. Vacca in Session 22, "Packaging for High Performance," circuit delay and off-chip
interconnect delays are more significant.\textsuperscript{12} Table 1 shows his comparison of interconnect delays in three media. Although the velocity of a signal on the chip is several times slower than off the chip, the short on-chip path length still makes it desirable to put serial stages on the chip.

VLSI design. In addition to the barriers set by physics, the design of a chip containing 150,000 gates—which is the five-year goal set by the Department of Defense’s VHSI Project—presents barriers of cost and time. According to W. M. van Cleemput of Stanford University (Session 1, “Design Automation for VLSI Systems”), at the current state of the art the cost of developing a 2000-gate chip is at least $200,000 and the development time is about one year.\textsuperscript{13} That amounts to over $100 per gate or, to be dramatic, more than $15 million for DOD’s VHSI chip. Obviously, it would take many years to expend that much money on a single closely coupled project.

The ways out are design philosophy and design automation. The first hopes to simplify design by moving the type of interconnect along a continuum from random to regular (i.e., from custom designs to structured designs) and by moving cell size along a continuum from variable to regular (i.e., from custom logic to gate arrays), thus encouraging the ability to make interconnect wiring more regular.\textsuperscript{14}

In the gate-array approach the diffusion layers are predesigned and preprocessed to form a regular structure of primitive logic elements, but the elements are not interconnected at this time. Later the connections necessary to implement a custom logic function are designed by the user and returned in a machine-processable form to the vendor who completes the interconnections in a final manufacturing operation. This approach, as used by IBM in the new 4300 processor, reduces the layout problem to the routing of connections in an otherwise fixed topology.

The gate-array approach seems feasible for applications in the 5000-to 10,000-gate range, in van Cleemput’s view, but he questions its applicability in the 100,000-gate VLSI range. Here a hierarchy of cells, macro-cells, and supercells may be necessary. Recently, for example, Motorola extended the gate-array approach to a functional array which it calls the Macrocell. This chip, in addition to various gate types, employs larger primitives, such as flip-flops, decoders, and full adders.\textsuperscript{15}

Carver Mead of Caltech and Lynn Conway of Xerox Palo Alto Research Center, who are in the final stages of preparing a text on VLSI design, have propounded a design style which emphasizes structuring a large design into functional cells and laying out the cells in a physical pattern in which each cell has the same pitch. This uniform spacing then permits the cells to be interconnected by what Gray calls orthogonalized wiring, as contrasted to the random interconnections required by irregular cell sizes or shapes.

In addition to the design simplification provided by relating functional design to physical design, Gray believes that the structuring of design allows design representations to be developed that will facilitate capturing design information.\textsuperscript{14} And that is the first step to design automation.

This area was the subject of a session on the requirements VLSI is placing on design automation. About a dozen existing DA systems were reviewed\textsuperscript{16} and papers were presented on two new systems, VISTA at Hughes Aircraft Company\textsuperscript{16} and DIAL at Microtechnology Corporation.\textsuperscript{17}

VLSI test. If the design is large and complex, test presents a similar barrier. At the present time, according to Linvill, “no sufficient programs exist for the test of integrated circuits of the VLSI class.” The hardware testing session, describing test generation methods for sequential circuits and microprocessors, is reported by Frank Mathur elsewhere in this issue.

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<th>MEDIUM</th>
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New architectures needed. The advent of VLSI is changing the design tradeoffs in computer architecture, Linvill points out. Signal paths are becoming more costly than switches. Memory and processing capability can be combined and distributed to the points where they are needed, leading to various parallel operation possibilities. The declining cost of logic elements provides the architect with what Linvill calls "element abundance." This abundance permits the microcomputer to become easier to use through the means of higher-level languages, error correction schemes, continual self diagnosis, and perhaps even self repair. "A perfectly operating machine with some imperfect elements is on the horizon," Linvill predicts.

Device-computer partnership. As more of the total computer disappears within the chip, the hitherto separate provinces of the semiconductor device engineer and the system designer are beginning to merge. At issue is how this combination of capabilities is to be organized. Can the semiconductor manufacturer integrate upward? Can the computer makers reach out for device expertise? Can National Semiconductor, to take a particular example, which has a computer plant in San Diego and chip facilities in Silicon Valley, bridge this geographic gap? Behind the organizations are people and behind the people, as Linvill sees it, are the universities which educate them. The coupling of VLSI and computers, he feels, is "likely to be done by new professionals rather than veterans." That would move the barrier to growth back to the university level. More likely, the vigor of the two fields will find many ways in which to bring partnerships into being.

Novel technologies

Although the concept of exploding technology is undoubtedly based primarily on the silicon revolution, the conference did go on to raise the question: Are fiber optics, the Josephson effect, or amorphous materials applicable to computers? The three speakers in this session (Session 14), replied, in a word, yes.

Fiber optics. Data links of this material are feasible today in computer and industrial applications, according to Delon C. Hanson of Hewlett-Packard’s Optoelectronic Division.18 During the past year use of this technology has expanded.

However, numerous problems still beset the new user. Solid information on design alternatives and cost/performance tradeoffs is sparse. Standards remain to be worked out. Data on long-term reliability in various environments is lacking. And, of course, many potential users still have to educate themselves in this new technology.

Nevertheless, the advantages of high data rate, noise immunity, and small physical size make fiber optics a technology worth the examination of the computer community.

Josephson junctions. Hollis L. Caswell recounted IBM's research experience with Josephson junction superconducting technology.19 For example, long Josephson junctions on 5-μm design rules have been designed, fabricated, and tested, with gate performance measured at 70 to 80 picoseconds. At 2.5-μm design rules, gates are anticipated to have only half this delay. Power dissipation would be less than 10 microwatts per gate.

The research laboratory's next step is to build a small prototype computer of some 6000 circuits and 150K bits of cache memory as a test vehicle. At the present stage of development this technology offers great promise, but it is tempered by high risk. Because only a small segment of the technical community is working in this field, the burden of surmounting a demanding set of tasks and reducing the technology to practice falls unfortunately on only a small number of researchers.

Amorphous materials. Stanford R. Ovshinsky has become widely known as the father of ovonic materials, some of which are now in use in products such as the Burroughs-ECD Ovonic 1024-bit nonvolatile 15-nanosecond bipolar read-write memory. Although silicon technology has been based on crystalline silicon, Ovshinsky developed an amorphous silicon-based alloy last year which "for the first time has greatly reduced states in the gap."20 Previously these states had kept amorphous materials from being used as control devices. In Ovshinsky's judgment, this new material can be appropriately doped, "opening up device applications that can permit new generations of control devices for computers."

Responsible growth

Because of exploding technology the computer industry has been able to supply continually improving performance at less actual cost. During the past decade of inflation, the industry has generally achieved better price/performance even as measured in inflating dollars. This record is the industry's most significant contribution to responsible growth.

Although part of the credit for this contribution rests with the major computer makers, another portion may be attributed to the plug-compatible vendors—a segment of the industry examined by a panel in Session 23, "Plug-Compatible Computers."

Program-compatible mainframes. In the past three years the concept of plug compatibility—program compatibility, really—has been extended from memory add-ons and peripherals to the mainframes themselves. Itel has installed about 300 systems manufactured by National Semiconductor. Amdahl is up to about 250 systems. Two Pi and Magnuson Systems announced program-compatible mainframes last year.

Now that IBM has moved a long way down the price/performance curve with its announcement of the 4331 and 4341 mainframes, have the PCM vendors been seriously wounded? Panel Chairman Whitcomb and John Bock of Itel, Richard Chueh of National Semiconductor, and Carleton Andahl of Magnuson Systems all seemed to agree that there was no indication of any blood loss.

Whereas all the panelists spent some time describing their companies and products, John Bock devoted most of his attention to the structure of the PCM industry. According to Bock, the industry depends upon the fact that program compatibility goes all the way back to the IBM series 360. The big computer company made a whole series of computers that operated on the same software structure and thus became the first program-compatible mainframe vendor. It stayed compatible with itself when it announced the 370 series in 1970, five years before the first competitive PCM, Amdahl, delivered its first computer. The same policy prevailed in the IBM 303x and 4300 mainframes.

The motivation behind this policy, said Bock, is the hundred of billions of dollars worth of compatible software out there. If IBM were to introduce a
truly revolutionary computer, its customers could switch to Itel, Amdahl, and the others who would still be compatible with the existing mass.

So, the market is not going away, Bock believes. Moreover, the independents are not naive about the moves IBM can make. The leading manufacturer is constrained by many of the same forces that its smaller competitors also feel. The PCMs realize full well that IBM over time will upgrade price/performance—exploding technology cannot be avoided. They know they will have to react to these improvements. When IBM announced the 303x series, for example, the PCM vendors soon announced new machines and price reductions.*

One of the keys to meeting future competitive moves is to keep the plug-compatible mainframes flexible and the way to do this is through microcode. Although IBM stays generally compatible each time it moves, it may add 10 to 14 instructions. Another key is to stay alert to the growth of main memory underscores the limitations of 24-bit addressing. It is confining to have to go out through an I/O channel every time a system needs more than 16 megabytes of space. Itel has a strategy in mind to implement 31-bit addresses, while retaining 24-bit address structures within regions, so as to avoid the necessity of massive software changes. Bock is sure IBM, Amdahl, and the others are thinking about this problem, too.

At present IBM seems to be pursuing two tacks. For one, it is making its announcements in small steps with the aim, in Bock’s opinion, of keeping the marketplace “churn.” If users are continually wondering what is coming around the corner next, they are reluctant to make long-term decisions. The easy decision is to stay with IBM.

The second tack is “to move the dollars around”—i.e., to reduce the relative income from hardware and increase it from software and firmware. (“Firmware” refers to routines that would in the past have been realized in software, as opposed to the basic microcode that drives the machine itself.) However, there is a limit to this strategy. If IBM moves too much income into software, it encourages competition in that market. In the upshot Bock expects to see a carefully tuned combination of software and firmware.

Medical costs. The health-care industry now expends almost 9 percent of the gross national product, up from less than 6 percent in 1966. The rise has many contributors—Medicare and Medicaid, more medical insurance, more complex medical procedures, and more technology. The question is whether the country wants to pay this rising bill. Session 2, a panel organized by Thelma Estrin, director of UCLA Brain Research Institute’s Data Processing Laboratory, addressed one aspect of the larger question: can computer technology help contain this cost?

The panelists agreed that computers are cost-effective in hospital administration and medical research, but took a range of positions on whether the computer can cut the cost of direct patient care. At one end of the spectrum Stanton A. Glantz, assistant professor of medicine and member of the Cardiovascular Research Institute at UC San Francisco, holds that “computer applications in clinical medicine often simply increase costs without improving clinical outcome.” Dr. Estrin disagrees. (In fact, it was Glantz’s development of his views in a Computer article[22] that led Estrin to organize this rebuttal.)

Richard Sneider of Technicon supported Estrin’s position to a degree. His experience is with a hospital-wide medical information system which Technicon has installed in a half-dozen hospitals. The system stores patient data for use by medical personnel, both doctors and nurses.

The only physician on the panel was Edmund Van Brunt, assistant director of medical methods research at the Kaiser-Permanente Medical Group. His experience has been with an automated multiphasic health testing facility, used to capture patient data. His judgment is that “for equivalent cost, computer technology makes medical information more useful and manageable.”

“Present medical data base systems suffer for lack of good design methodology and do not utilize recent advances in data base management theory and methods,” according to Anthony I. Wasserman, assistant professor of medical information science, UC San Francisco, and an expert on software design methods. Considerable cost improvement is possible, but Wasserman still tends to agree with Glantz, saying, “Computer technology cannot contain the cost of health care because the costs are determined essentially by economics, politics, medical practice, and other factors which computer technology does not influence.”

Panel Chairman Estrin believes that the effective application of information technology to the increasingly complex patient data generated by advancing medical knowledge is a “social imperative.” At present, patient information often resides in scattered, multiple-paged records that have the character of an unorganized “scrap book.”

In this form the physician has difficulty bringing all the data that has been taken at one time or another to bear on the series of decisions that govern the care of the patient. The unedited records fail to facilitate care over a long period of time by different doctors. They hamper research studies of the outcome of treatment.

LSI technology, state-of-the-art input and display devices, data base management techniques, the personal computer—all represent aspects of computer technology that Dr. Estrin views as components of potentially successful health care systems. To make them actually effective in daily practice requires the understanding cooperation of the using physicians. Government can help, she feels, by sponsoring research, encouraging professional training in this area, and, as the largest purchaser of health care services, by encouraging the transfer of this technology to practical application.

Computerized medical information systems can not only eventually reduce costly paperwork, she concluded, but they can improve patient care—the ultimate goal of the whole health care delivery system.

Still with us, “It seems almost axiomatic that software is never produced on time, never meets specification, and always exceeds its estimated cost.”[23] That was the opening sentence of Robert M. McClure’s paper over 10 years ago at the first NATO Software Engineering Conference. He used it again at COMPON because it still applies.
McClure estimates that upward of one-half million people do at least some programming on a regular basis. Fewer than 20 percent of them, however, were in the field in 1968. If the software field can’t have exploding technology, it can have explosive growth.

As a result of this growth, the traumas of programming development in the 1960s are only distant events to most programmers today, on a par with the “Pop, what did you do in the war” generation.

But all is not hopeless. McClure went on to say that software can be produced on time; it can be managed successfully; programmers can have adequate tools; their productivity can improve; property rights in software can be protected. Although, he didn’t explain in detail how these tasks are to be accomplished, it does seem clear that those who are moved to apply themselves to these problems will still have to attend the tutorials and short courses, read the books, peruse the literature, and work hard.

Acknowledgments

Dean Brown, general chairman, and Fred Buelow, program chairman, helped me place the conference in perspective.

References