ADVANCE PROGRAM
The 6th Annual International Symposium on
COMPUTER ARCHITECTURE
April 23-25, 1979
Sponsored by
ACM SIGARCH And IEEE COMPUTER SOCIETY TCCA
at
PHILADELPHIA MARRIOTT
CITY LINE AVENUE
PHILADELPHIA, PENNSYLVANIA

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TUTORIAL
Monday, April 23, 1979 — 1:5 PM
Data Base Computers
Professor D.K. Hsaio, Ohio State Univ.
Dr. G.A. Champine, Sperry Univac

An overview is presented of past and present advances in Data Base Computers. Advantages and disadvantages are presented in a general framework, and then in the context of various applications. Specific projects or implementations are reviewed in detail, along with strengths and weaknesses of each. Finally, projections for the future of the Data Base computer technology are made.

PROGRAM
Tuesday 8-9 am
Late Conference Registration

Tuesday 8:10-30 am
Opening Remarks: Barry R. Borgerson, General Chairman;
E. Douglas Jensen, Program Chairman
Keynote Address: Richard L. Gehring, President, Sperry Univac
Div. of Sperry Rand Corp.

Tuesday 10:45—12:15
SESSION I Chairman—Harold Stone, U. Mass.
“A Concurrent Computer Architecture and a Ring-based Implementation”
Edward P. Farrell, Noordin Ghan, Philip C. Treieaven, U. of Newcastle Upon Tyne
“Designing Pipeline Architectures Using On-Line Algorithms”
Robert Michael Owens, Mary Jane Irwin, Pennsylvania State University
“Architectural Implementations of Abstract Data Type Implementation”
Virgil D. Gilgor, U. of Maryland

Tuesday 1:15—2:45
SESSION II Chairman—Dan Siewirot. Carnegie-Mellon
“A New Approach to an Adaptive Computer - An Automatic Recovery Mechanism to Prevent the Occurrence of Subtract Errors”
Ken Sakamura, Koochi Nakano, Yoshio Kato, Hideo Aiso, Keio University.
“Overview of the ARCADE System”
A. Brandwajn, J. A. Hernandez, R. Joly, and P. Kruchten, Ecole Nationale Superieure des Telecommunications
“A Proposal for an Architecture with Many Operand Registers to Efficiently Execute Block-Structured Languages”
Roger B. Dannenberg, Case Western Reserve U.

Tuesday 3:00—4:30 (Parallel Sessions)
SESSION IIIA Chairman—George Champine, Sperry Univac
David Hsiao, Ohio State University
DATABASE PROCESSOR PANEL
P. Bruce Berr, Syracuse University
George P. Copeland, TEKTRONICS
David J. DeWitt, University of Wisconsin
Harvey A. Freeman, Sperry Univac
James A. Tillinghurst, MRI Company

SESSION IIIB Chairman—Jacques Lenfant, University of Rennes
“A Multiprocessor Architecture for Video Graphics”
Henry Fuchs, U. of North Carolina; Brian W. Johnson, U. of Texas at Dallas
“A Bit-Slice Cache Controller”
B. D. Ackland, Bell Laboratories

Tuesday 4:30—6:00
ACM SIGARCH/IEEE C.S. TCCA Business Meeting (Open)

Tuesday 6:00—7:00
Conference Reception

Tuesday 7:00—10:00
Conference Banquet—Presentation of first IEEE/ACM Eckert-Mauchly
Computer Architecture Award by Dr. J. Presper Eckert and Dr. John W. Mauchly.

Wednesday 8:15—9:45 (Parallel Sessions)
SESSION IVA Chairman — T.C. Chen, IBM
“Experiments on a Tree Organized Multicomputer”
J. Archer Harris, U. of Southern Illinois, David R. Smith, State U. of New York at Stony Brook
“Design Considerations for the VLSI Processor of X-tree”
David A. Patterson, E. Scott Fehr, and Carlo H. Sequin, U. of California
“FLATS, a Machine for Numerical, Symbolic and Associative Computing”
Elchi Goto, U. of Tokyo, Tetsuo Ida, Institute of Physical and Chemical Research, Japan, Kei Hiraki, U. of Tokyo

SESSION IVB Chairman—Hideo Aiso, Keio U.
“Some Simplified Performance Modeling Techniques with Applications to a New Ring-Structured Microcomputer Network”
J. Spragins, T. Lewis, Oregon State U., H. Jafari, National U. of Iran
“A Performance Comparison of Optimally Designed Computer Systems with and without Virtual Memory”
Kishor S. Trivedi, Timothy M. Sigmon Duke University
“A Modeling Approach and Design Tool for Pipelined Central Processors”
T. K. Agerwala, K.M. Chandy, D. E. Lang, U. of Texas at Austin

Wednesday 10:00—11:30
SESSION V Chairman—Bob Sugarman, IEEE Spectrum
16-BIT MICROPROCESSOR PANEL
Bill Polzman, Intel
Edward Stritter, Motorola
Bernard Peuto, Zilog

Wednesday 12:30—2:00 (Parallel Sessions)
SESSION VIA Chairman—Wes Chu, UCLA
“Dynamic Function Exchanging Mechanism in Poly-Processor System”
“The Architecture of Sperry Univac 1100 Series Systems”
“An Efficient Time-Shared Link Processor for Supporting Communication in Parallel Systems with Dynamic Structure”
H. K. Rughbati, U. of Saskatchewan

SESSION VI B Chairman—Mark Franklin, Washington University
“Packet Switching in Banyan Networks”,
Anand R. Tripathi, G. Jack Lipovski, University of Texas at Austin
“On the Processor-Memory Interconnections for Multiprocessors”
Janak H. Patel, Purdue University
“Proof of the Equivalent Realizability of a Time-Bound Arbiter and a Rent-Free Inertial Delay”
B. I. Strom, Bell Laboratories

Wednesday 2:15—3:45 (Parallel Sessions)
SESSION VIIA Chairman—Terry Welch, Sperry Research
“Design Issues in the Development of a Modular Multiprocessor Communication Network”
“Experimental Polyprocessor System - Architecture and Functional Distribution”
Mamoru Maekawa, et. al.; Toshiba Research and Development Center
“Experimental Polyprocessor System - Firmware and Processors”
Mamoru Maekawa, et. al.; Toshiba Research and Development Center

SESSION VIIB Chairman—Dick Kain, U. Minn.
“A Microprocessor Controlled Asynchronous Circuit Switching Network”
Tse-yun Feng, Chauan-In Wu and Dharma P. Agrawal, Wayne State U.
“Performance Enhancement of SISD Processors”
W. G. Rosocha, E. S. Lee, U. of Toronto
“An Emulator Network for SIMD Machine Interconnection Networks”
S. Diane Smith, H. J. Siegel, Purdue U.

Wednesday 4:00 Buses Leave for Airport