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R78-59—Kim, K. H., “Programmer-Transparent Coordination of Recovering Parallel Processes” (61 pp., University of Southern California, Los Angeles, California)

This paper presents a new approach to coordination of cooperating parallel processes, each capable of error detection, rollback, and retry. These are specified by a well-structured language construct called recovery block. Coordination of processes is needed to prevent a disastrous avalanche of process rollbacks. In contrast to the previously studied approaches that require the program designer to coordinate the recovery block structures of interacting processes, the new approach relieves the program designer of that burden.


The Monitor Command System is a 1K-byte monitor. MCS is designed to be system-independent, and it has been implemented on a 8080-based microcomputer system. It provides a number of system utilities, such as input/output routines, and a set of user commands which provide memory manipulation, program loading, and program debugging facilities.


It is well-known that static redundancy techniques are very efficient against intermittent (transient) faults, which constitute a large portion of logic faults in digital systems. However, very little theoretical work has been done in evaluating the reliability of modular redundancy systems which are subject to intermittent malfunction occurrences. This paper presents a statistical model for intermittent faults and uses it to analyze the reliability of NMR systems in mixed intermittent and permanent fault environments.


In determining an FFT length N in convolution applications, computation times that are proportional to N, as well as those that are proportional to Nlog(N), may be significant factors. Such factors are easily taken into account and the relevant optimization problem can be solved with a small calculator for arbitrary values of the parameters, including the radix. The extension to the multi-dimensional case is straightforward except for one standard difficulty.

R78-63—Magliveras, S. S., Y. S. Shen, and N. Tsolas, “On the Number of Classes Under Permutation Equivalence of q-valued n x m Incidence Matrices” (11 pp., State University of New York, Oswego, New York)

Let Ω be the collection of all n x m matrices with entries from a set F of cardinality q. Two matrices A and B in Ω are considered equivalent if there are permutation matrices P, Q such that A = P* • B • Q. In this paper we explicitly calculate the number of equivalence classes f_i (n,m), in Ω, via an application of a well-known lemma of W. Burnside.

R78-64—Dalal, Y. K., “Broadcast Protocols in Packet-Switched Computer Networks” (275 pp., Stanford University, Stanford, California)

This report investigates the design and analysis of broadcast routing algorithms for use in store-and-forward packet-switched computer networks using reliable and efficient protocols; it examines five alternatives to transmitting separately addressed packets from the source to the destinations. An outcome of the investigation of broadcast routing algorithms is the formulation of two distributed (parallel) algorithms for constructing minimal spanning trees. The author believes that these algorithms are the first of their kind. The formulation of
such algorithms has made the problems affecting the design of distributed algorithms in network environments clearer. These minimal spanning tree algorithms can be used in broadcast routing, as well as other networks like the Packet Radio Network.

R78-65—Snow, E. A. and D. P. Siewiorek, "Impact of Implementation Design Tradeoffs on Performance: The PDP-11, A Case Study" (78 pp., Carnegie-Mellon University, Pittsburgh, Pennsylvania)

This paper studies design tradeoffs occurring in eight different DEC PDP-11 implementations and the effects of the tradeoffs on performance. An archetypal PDP-11 implementation is described followed by model-specific variations. These variations represent the design tradeoffs and are grouped by areas—i.e., circuit technology, control unit, and data paths. Analysis of the design tradeoffs, the paper presents two design methodologies. A top-down approach uses microcycle and memory read pause times to account for 90 percent of the variation in processor performance. A bottom-up approach uses relative frequency of functions to determine the impact of specific tradeoffs on performance.

R78-66—Glanc, A., "A Note on Some Problems in Robotologic" (4 pp., State University of New York, Potsdam, New York)

Four requirements of robotologies—derived from considerations of some assumed robot’s limitations—are briefly discussed and formulated. It is assumed that the robot has to gain a knowledge of his particular environment, having only partial information about all possible environments.


This thesis describes a word screening and scanning feature in the experimental on-line full-text Eureka retrieval system. Given any specified collection of documents in the data base, the feature can reduce words within the set to distinct occurrences, screen out insignificant words, provide distribution statistics of the words, and based on these statistics, enable users to selectively look at alphabetical listings of these words. This feature saves users considerable efforts in narrowing their search. Also, by using the feature to generate word arrays which characterize documents, documents in the data base can be clustered to workable sizes for generating thesauri by statistical methods.

R78-68—Hammerstrom, D. and E. S. Davidson, "The Use of Second Order Memories to Reduce Memory Addressing Overhead" (42 pp., Cornell University, Ithaca, New York)

This paper discusses the process of generating memory addresses by computer programs and presents a method for making that process more efficient. The approach taken is to separate program execution into a computation process and an addressing process. The addressing process generates the memory reference stream for the computation process and for itself as well. The memory reference stream of the computation process can then be modeled probabilistically and its information content derived. It is shown that not only does the addressing process place a great load on the system, but that much of that load is unnecessary. Two examples of second order memories are presented and analyzed. Their use not only reduces the addressing overhead inherent in computer program execution, but also significantly reduces bandwidth requirements between the CPU and the memory system.

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