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R78-42—Trivedi, Kishor S., and Robert A. Wagner, "A Decision Model for Closed Queuing Networks" (30 pp., Duke University, Durham, North Carolina)

This paper considers the cost-performance optimization of systems that can be modeled using a closed queuing network. The system throughput is the objective function to be maximized and the speeds of the servers are the decision variables. A rich class of nonlinear cost functions is considered. The paper shows that any local optimum of the optimization problem is also a global optimum. It also shows that the cost constraint is active and that the method of Lagrange multipliers can be used to solve the problem efficiently.


This paper discusses the overall design of a Plato lesson sequence, particularly that of the Pascal series, a sequence intended for introductory computer science courses. It lists the topics and concepts covered by each lesson of the sequence, and discusses some general considerations in writing Plato lessons.

R78-44—Zaks, S., and D. Richards, "Generating Trees and Other Combinatorial Objects Lexicographically" (19 pp., Report No. UIUCDCS-R-77-903, University of Illinois, Urbana, Illinois)

The authors show a one-to-one correspondence between all the ordered trees that have \( n + 1 \) leaves and \( n \) internal nodes with \( k \) sons each, for \( i = 1, \ldots, t \), (hence \( n_i = \Sigma(k_i - 1)n_i) \), and all the lattice paths in the \( (t + 1) \)-dimensional space, from the point \( (n_t, n_{t-1}, \ldots, n_1) \) to the origin, which do not go below the hyperplane \( x_0 = \Sigma i|k_i - 1|x_i \). Procedures for generating these paths, and thus the ordered trees, are presented and the ranking and unranking procedures are derived.


Let \( c, d, d_0, \ldots, d \) be integers such that \( 1 < d < d_0 < \ldots < d < c \). Let \( t \) denote the sum \( (d_1 + \ldots + d_i) \). Given \( c \) distinct colors, the authors order the \( (d_i) \) subsets of \( d \) colors, \( (d_2) \) subsets of \( d_2 \) colors, \( \ldots \), and \( (d) \) subsets of \( d \) colors in some arbitrary manner. Let \( G_0, G_1, \ldots, G_c \) be graphs. The \( (d_1, d_2, \ldots, d_c) \)-chromatic Ramsey number for \( G_0, G_1, \ldots, G_c \), denoted \( R_{d_1, d_2, \ldots, d_c}(G_0, G_1, \ldots, G_c) \), is defined to be the least integer such that if the edges of the complete graph \( K \) are colored in any fashion with \( c \) colors, then for some \( i \) the subgraph whose edges are colored with the \( i \)th subset of colors contains a \( G_i \). This paper investigates the case \( R_{c, \ldots, c}(G_0, G_1, \ldots, G_c) \).

R78-46—Rosenthal, Arnie, "Hard Computational Problems in Reliability Theory" (18 pp., University of Michigan, Ann Arbor, Michigan)

This report applies results from the theory of computational complexity to a number of reliability computations on combinational circuits, i.e., on fault trees, and on networks. First, the well known "NP-hard" class of problems, which almost certainly have no fast solution algorithms, is presented. The paper then shows that the problem of computing the reliability of many systems, or even approximating their reliability to within a constant factor, is difficult enough to be in this class. These results strongly suggest that no practical algorithm exists which will always solve the problems discussed in this paper.

A collection of over 2600 technical papers (some refereed, some not), covering the full range of computer system design and maintained by the Computer Society as a service to the information processing community.
R78-47—Chong, Fay, Jr., "Execution Time Analysis for Real-Time Microcomputer Programs" (263 pp., University of California, Berkeley, California)

This paper presents some tools for the development and analysis of real-time programs, including a programming language and a technique for evaluating and testing worst-case program execution times. The most outstanding feature of this analysis technique is that the source program structure is preserved during translation. This structural information is used to direct the worst-case execution-time analysis. The execution-time information is then reflected back onto the syntactical statements of the source program. The real-time programming language, called PLRTC (Programming Language for Real-Time Microcomputers), requires that the source program be composed of only sequential, alternative, and iterative control structures. The PLRTC compiler translates the source code into an intermediate language. Execution times are then assigned to the instructions of the compiled program, and the intermediate object code is analyzed by the execution-time analysis program.


This paper describes a metanotation for defining the syntax and semantics of a programming language in a rigorously formal manner. Definitions are operational: A semantic definition is a set of string transformation rules that operate on concrete representations of programs and their environments. The formalism is simple and easy to learn, and produces relatively readable language descriptions. To illustrate the formalism, and to facilitate comparison with other metalanguages, the paper presents a formal definition of the programming language ALGOL. The method is compared in detail with the W-grammar approach, and some techniques for verifying the consistency of definitions are discussed.

R78-49—Kim, Won, "Relational Data Base System Implementations—A Survey" (66 pp., Report No. UIUCDCS-R-78-913, University of Illinois, Urbana, Illinois)

This paper surveys the overall structure and design of some of the prototype relational data base systems frequently referenced in the literature, and then examines in some detail some interesting approaches that have been taken in implementing various requisite features for a comprehensive relational data base system.

R78-50—Dervisoğlu, Bülent, "Reliable Input Synchronizers and Flip-Flops" (28 pp., University of Connecticut, Storrs, Connecticut)

Synchronous sequential circuits which also receive asynchronous inputs are subject to indeterminate behavior. Using synchronizers to synchronize asynchronous input changes with the system clock is a possible solution to the problem. However, due to the unreliability of existing synchronizers this approach does not guarantee fail-safe operation. It may also be possible to treat the circuit as an asynchronous sequential circuit, with the clock as another input. This approach also fails due to the effects of runt pulses on circuit behavior, since there is no known way of completely filtering them out. This paper addresses the problem of designing reliable synchronizers. It shows that a very simple OR latch can be constructed which will not be affected by runt inputs. The use of the OR latch in constructing an input synchronizer is illustrated along with the design of a clocked SR flip-flop and a JK flip-flop. The proposed circuits can be constructed using IC gates and switching diodes, with total monolithic integration also possible.

R78-51—Plavsic, Vojin, and Per-Erik Danielsson, "A New Method for the Evaluation of Boolean Functions" (32 pp., Linköping University, Linköping, Sweden)

This paper presents methods for iterative evaluation of Boolean expressions suitable when the input variables appear in sequence, e.g., in sequential searching and matching. The sum-of-product form is assumed and the clue is to compute the values of the products partially for each new variable being defined. The authors show that the additive use of an expression for the complementary function can result in a faster evaluation. The method proves to be extendible to multilevel expressions.


Multiprocessor systems are characterized by the types of processors in the system. Some multiprocessor systems consist of identical general-purpose processors which share the input job load under the control of the job scheduler. Other multiprocessor systems consist of special-purpose processors, each of which is designed to execute a particular type of job. Both types of multiprocessor systems are modeled queueing-theoretically, and their performance is evaluated to determine their relative architectural merits. In the case of the multiprocessor system with special-purpose processors, the optimal architecture is discussed.


The author proposes a machine organization for the fast processing of Snobol programs. Measurements of Snobol programs are given to support various choices. Since pattern matching is a major time consumer in Snobol, special hardware is proposed for it. Several alternative designs were studied in detail and cost-effectiveness measures are given for these.

R78-54—Chang, Donald Yi-Chung, "Further Results Regarding Multiprocessor Systems" (238 pp., Report No. UIUCDCS-R-77-908, University of Illinois, Urbana, Illinois)

The recent developments of inexpensive but powerful LSI microprocessors and high-density semiconductor memory chips have led to the design of large computer systems containing a large number of processors and memory modules. Many systems have been built with many processors interconnected with a large number of memories, e.g., the Prime system, the C.mmp system, and the Tandem NonStop system. All these systems have one common feature, i.e., increased system throughput by simultaneous operation of several processors. Each system has a different architecture with its own advantages and disadvantages. This thesis examines various questions associated with the different architectures in order to get a better understanding of multiprocessor system design. Because these systems are highly complex, simulation techniques are used to collect the data needed to answer the questions. The author gives a detailed description of the simulator and presents simulation results, as well as some logic design problems concerning the real system design.

R78-55—Hansen, Per Brinch, and Jorgen Staunstrup, "Specification and Implementation of Mutual Exclusion" (22 pp., University of Southern California, Los Angeles, California)

This paper presents a constructive approach to the problem of specifying, implementing, and verifying operations that will give concurrent processes exclusive access to a resource. The method eliminates the need for auxiliary variables and establishes the correctness of a whole class of solutions to the same problem. The solutions are derived directly from the specifications, using a language construction called guarded regions. Several new solutions to well-known exclusion problems are presented.

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The speeds of devices constituting a computer system influence system throughput. This paper determines the speeds which will maximize such throughput, given a fixed budget. The system composed of a central processor and peripheral devices is modeled as a closed queueing network of exponential servers. This problem is formulated as a nonlinear optimization problem where the objective is to maximize throughput subject to a nonlinear cost constraint. Individual device costs are represented by continuous power functions of device speed. Main memory costs are considered in terms of the degree of multiprogramming. The Lagrange multiplier technique is employed to set up a system of simultaneous nonlinear equations which are solved to produce the optimal solution.


This report presents abstracts of reports on currently completed research projects, status summaries of current projects, and explanations of new projects at the Information Engineering Laboratory of the Department of Computer Science at the University of Illinois at Urbana-Champaign.


The elementary school is well-suited for introducing computer concepts and the basics of programming. To find the best way of teaching programming to children, the process by which programming is learned should be analyzed; however, little has been done to study the process of learning to program. This thesis describes PAL (Picture Algorithm Language), a programming language designed for very young children, which is then used as a means of studying the process of learning to program. Tests in which several children learn to write computer programs are detailed. Also included are observations from these tests as to which concepts are easy and which are difficult to learn. Finally, some suggestions are made for teaching children how to program.


Vicent J. Giardina, IEEE Manager of Continuing Education, 445 Hoes Lane, Piscataway, NJ 08854; (201) 981-0060, ext. 177.

European Economic Community Advanced Course on the Design of Distributed Processing Systems: June 26-July 7, Nice, France.

D. Neel, IRIA—B.P. 105, 78150 Le Chesnay, France.


Distributed Data Processing: June 19-22, San Francisco, California.

AIIE Computer and Information Systems Division, PO Box 3727, Santa Monica, CA 90403; (213) 450-0500.

Charge Transfer Devices—Theory and Applications: July 10-14, Washington, DC. Fee: $495.


The American University, Office of Summer Sessions and Special Sessions, Massachusetts and Nebraska Avenues N.W., Washington, DC 20016; (202) 686-2697.

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CCD and SAW—Basic Theory and Application to Communications, Radar, and Signal Processing: July 31-August 4, Lake George, New York.

Office of Continuing Studies, Rensselaer Polytechnic Institute, Troy, NY 12181; (518) 270-6442.


Structured Design and Programming Workshop: June 19-23, Washington, DC. Brandon Systems Institute, 4720 Montgomery Lane, Bethesda, MD 20014; (301) 988-8611.


Datapro Research Corporation, 1805 Underwood Blvd., Delran, NJ 08075; (609) 764-0100.


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