Standards for Microprocessors

Robert G. Stewart
Stewart Research Enterprises

The rapid acceptance of microprocessors for sophisticated control and computation has focused attention on the need for microprocessor standards. One positive response to this problem has been the creation of the IEEE Computer Society's Microprocessor Standards Committee in August 1977. Operating under the aegis of the Computer Standards Committee, the committee is aimed at developing software and hardware standards for microprocessors and related equipment.

The tasks initially undertaken were selected primarily on the basis of urgency. In the software standards area, the topics are microprocessor instruction sets and mnemonics, relocatable code format, and floating point format. The main initial hardware issue is the standardization of the existing de facto busses: Intel's Multibus, National's Microbus, and the S-100 Bus.

Software Issues

The software tasks are being studied by a subcommittee chaired by Tom Pittman, a microprocessor software consultant. (Tom is also acting as the representative of the Homebrew Computer Club.) An initial draft of a proposed microprocessor instruction set and mnemonics has been prepared by Wayne Fischer of Kaiser Electronics. The draft proposes the rule that instructions be named consistently by one convention (insofar as possible), namely:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Verbs</th>
<th>Operators</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source</td>
<td>Direct</td>
<td>Indirect</td>
</tr>
<tr>
<td>or</td>
<td>Object</td>
<td>Object</td>
</tr>
<tr>
<td>or</td>
<td>or</td>
<td>Source</td>
</tr>
<tr>
<td>or</td>
<td>or</td>
<td>Destination</td>
</tr>
</tbody>
</table>

which corresponds to the normal word order in the English language. For example, we say: "Put the bread on the table," rather than "Put on the table the bread."

The widespread use of microprocessors to accomplish tasks formerly done with TTL logic has meant that programming in assembly-language code must be done by a much larger number of persons than previously required. Many computer hobbyists are working at this level. By standardizing instruction sets (to the extent permitted by architecture) and mnemonics, we can simplify the process of learning assembly-language programming for both student and instructor. In addition, code developed for one microprocessor will be more easily understood and more apt to be used by someone whose experience was obtained on a different microprocessor.

The converse of this situation is particularly evident in the hobby magazines today, where an article with an elaborate program developed for one microprocessor is essentially unintelligible to someone used to working with a different microprocessor. Even where the entire instruction set of one microprocessor is included as a subset of another one, a different list of mnemonics may have been established by the manufacturer for instruc-

March 1978
tions that are themselves common and compatible. Furthermore, instruction sets have been copyrighted by microprocessor manufacturers in order to preserve their proprietary interests. Consequently, independent software organizations and timesharing computer services have been forced to prepare their own mnemonic sets for assemblers and cross-semblers, thus leading to a multiplicity of mnemonics for even one microprocessor. These are some of the cogent reasons for establishing a standard instruction set and mnemonics for microprocessors.

The reasons for creating standards in other software areas, such as relocatable code format and floating-point formats, are based on both software and hardware considerations. Portability of software modules between operating systems and hardware environments would certainly be enhanced. Forcing the need for standards even harder is the fact that semiconductor chip manufacturers can now put floating-point arithmetic processors into silicon and, in the future, will be able to put entire high-level language interpreters and compilers, assemblers, and operating systems with relocatable loaders into water form. In fact, it is the absence of these standards which is hampering the making of such wafers today.

**Hardware issues**

The hardware tasks of the Microprocessor Standards Committee are being carried out in a subcommittee chaired by Gordon Force of National Semiconductor. The decision has been made to concentrate initially on nailing down the existing de facto busses. The S-100 bus, established by MITS in 1975 for its Altair 8800 computer which used the Intel 8080 microprocessor, is the most widely used of all microprocessor busses; estimates of the number of mainframes using it range from 30,000 to 100,000. (Some computer hobbyists regard the Altair as the world’s first digital computer!) A number of new companies came into existence to provide memory, I/O, and other boards to plug into the Altair bus. As a result the bus was adopted early on as the common denominator of the burgeoning personal and small-business computer industry.

Moreover, designers proceeded to implement CPU boards with other microprocessors such as the Z80, 6800, 2650, bipolar bit slice, etc. Unfortunately, these devices do not necessarily have the same clock, timing, and control characteristics and signals as the 8080.

In view of the fact that the original MITS documentation for the Altair had no detailed timing and control specification for the bus, one can only conclude that the original Intel 8080 timing specification was presupposed. The conflict of timing problems among refresh rates of dynamic memories, DMA floppy disk controllers, wait states, access times, non-8080 processors, etc., has led to severe incompatibility problems between various boards and systems, all claiming to be S-100 bus compatible.

A draft of timing, control, and DMA protocol standards for the S-100 bus has been prepared by George Morrow of Thinker Toys and Howard Fullmer of Parasitic Engineering. All timing of signals is referenced to the phase 2 clock. Any device, board, or system claiming to be a bus master will be required to generate a fundamental subset of the S-100 bus signals within the timing tolerance. This standardization effort should ease the problems that have arisen with S-100 bus equipment, making it a viable bus for future hobby and small-business systems. The industrial busses, such as the Intel Multiplex used on the Intellonic development systems, have benefitted greatly by having a carefully thought out timing and control specification available initially. Also, they use negative true logic, which is a faster and cleaner transition in silicon devices. As new microprocessors become available with higher frequency clocks and shorter cycle times, new busses that pay more care to shielding, transmission characteristics, active termination, and active motherboards will be needed.

**Future plans**

Later the Microprocessor Standards Committee will propose standards for use in the small business and personal computer field.

The dynamic nature of the microprocessor field is in itself a strong argument for prompt and diligent action. To that end, committee meetings are being held on the second Thursday evening of each month at the Stanford Faculty Club, Stanford University, Palo Alto, California. Anyone wishing to participate should call or write the committee chairman, Robert G. Stewart, 1658 Belvoir Dr., Los Altos, CA 94022, (415) 941-6699 evenings.