ADVANCE PROGRAM
The 5th Annual Symposium on
COMPUTER ARCHITECTURE
April 3 - 5, 1978
SPECIAL DESIGN AUTOMATION TUTORIAL
April 3, 1978
Sponsored by
ACM SIGARCH and IEEE COMPUTER SOCIETY and DIGITAL SYSTEMS LABORATORY, STANFORD UNIVERSITY
at
RICKEYS HYATT HOUSE
PALO ALTO, CALIFORNIA

PROGRAM

MONDAY — April 3
Conference registration: 7-10 p.m.

TUESDAY — April 4
Late conference registration: 8:30 a.m.
Keynote Address: Robert N. Noyce, Chairman of the Board, INTEL Corp.

Session 1. Special Purpose Processors
Chairman: Alvin Despain, University of California at Berkeley
“A Digital Signal Processor for Real Time Generation of Speech Waveforms,” Glen S. Miranker, MIT
“Hardware Algorithms for Nonnumeric Computation,” Amar Mukhopadhyay, University of Iowa
“Design Considerations in an Optical Arithmetic Unit,” Alan Huang, Stanford University
“A Pipelined Mantissa Processing Unit for Division,” Mary Jane Irwin, Pennsylvania State University

Lunch

Session 2. Data Base Architectures
Chairman: David K. Hsiao, Ohio State University
“Architectural Features of CASSM: A Context Addressed Segment Sequential Memory,” G. J. Lipovski, University of Texas
“Rotating Memory Processors for the Matching of Complex Textural Patterns,” Lee Hollaar, University of Illinois
“The Design of a Database Machine with Large On-Line Storage,” Krish Kannan, Ohio State University

Session 3. Panel Discussion
“LSI Impact on Future Computer Business Strategy”
Moderator: Prof. Edward J. McCluskey, Director, Digital Systems Laboratory, Stanford University
Panelists: Paul C. Ely, Jr., Vice-President and General Manager, Computer Systems Group, Hewlett-Packard Co.; Robert N. Noyce, Chairman of the Board, INTEL Corporation; Dr. Federico Faggin, President, Zilog Inc.; Dr. Herbert Schorr, Manager of Systems Technology, IBM Research
Banquet: Speaker, Prof. Richard Hamming, Dept. of Computer Science, Naval Post Graduate School, Monterey, California

WEDNESDAY — April 5
Session 4. Language-Oriented Architectures
Chairman: Elliot Organick, University of Utah
“High Level Language Oriented Hardware and the Post-von Neumann Era,” H. J. Burkle, A. Frick, and Ch. Schlier, Universität Freiburg
“A Hardware Architecture for Controlling Information Flow,” Harry J. Saul and Israel Gat, IBM
“Computer Architecture for Correct Programming,” K. Berkling, Institute for Information Systems Research, Bonn, Germany

Session 5. Algorithms and Analysis
Chairman: Harold S. Stone, University of Massachusetts
“Selection of Microprocessor Equipment,” Edgar Maymon and Daniel Tabak, NASA-Langley Research Center
“Analysis of a Multiprocessor System with a Shared Bus,” L. L. Kinney, University of Minnesota, and R. G. Arnold, Honeywell Systems and Research Center
“Decentralized Parallel Algorithms for Matrix Computation,” Rajani M. Kant and Takayuki Kimura, University of Delaware
“An Analysis of the Cray-1 Computer,” Richard L. Sites, University of California at San Diego

Lunch

Session 6. Reliability
Chairman: Jack Goldberg, SRI International
“Storage Concepts in a Software-Reliability-Directed Computer Architecture,” Glenford J. Myers, IBM Corporation
“An Approach for a Fault-Tolerant System Architecture,” L. Boi and P. Michel, CERT/DERI, France
“Structure of an Efficient Duplex Memory for Processing Fault-Tolerant Programs,” K. H. Kim, University of Southern California, and C. V. Ramamoorthy, University of California at Berkeley
Session 7A. Recent Advances 1
Chairman: Bernard Peuto, Zilog Inc.

“An Approach to Using VLSI in Digital Systems,” Terry Welch, Sperry Research Center, and Suhas Patil, University of Utah
“X-Tree: A Tree Structured Multi-Processor Computer Architecture,” Alvin M. Despain and David A. Patterson, University of California at Berkeley
“Description and Simulation of Microcode Execution,” Alice C. Parker and Andrew Nagle, Carnegie-Mellon University
“Intelligent Magnetic Bubble Memories,” Mario Jino and Jane Liu, University of Illinois
“Data Structure Architectures – A Major Operational Principle,” W. K. Gilo, Technical University of Berlin, and H. K. Berg, University of Minnesota
“DIRECT – A Distributed Computer Architecture for Supporting Relational Data Base Management Systems,” David J. DeWitt, University of Wisconsin
“The PDP-11: A Case Study of How NOT to Design Condition Codes,” Robert D. Russell, University of New Hampshire
“Hardware Support for Concurrent Programming in Loosely Coupled Multiprocessors,” H. K. Reghbati and V. C. Hamacher, University of Toronto

Session 7B. Recent Advances 2
Chairman: Gary Tiaden, Sperry-Unixac Corporation

“Effects of Various Memory Configurations on System Performance,” Faye A. Briggs, Purdue University
“Study of SIMD Interconnection Networks,” S. D. Smith and H. J. Siegel, Purdue University
“Reliable Synchronization of Redundant Systems,” Daniel Davies, Stanford University
“The Effects of CPU I/O Overlap on Computer System Configurations,” Don Towsley, University of Massachusetts
“The Effectiveness of Buffered and Multiple Arm Disks,” Alan Jay Smith, University of California at Berkeley
“Pipelines with Internal Buffers,” Janah H. Patel, Purdue University

Tutorial
Monday, April 3, 1978
Computer-Aided Design Tools for Digital Systems

Registration
Conference registration includes a copy of the Proceedings, 2 continental breakfasts, 2 lunches, one banquet, and 4 coffee breaks. The student registration includes a copy of the Proceedings, and 4 coffee breaks.
Refunds requested before March 10, 1978 will be honored.

Please check appropriate registration categories, enclose check payable to “5th Computer Architecture Symposium,” and mail to:
Roy C. Ogus
Xerox SDD
3333 Coyote Hill Road
Palo Alto, CA 94304

Accommodations
To confirm your room reservation, Rickeys Hyatt House Hotel must receive this form and your deposit by March 10, 1978.

Please complete this form, ENCLOSE deposit to cover first night, and mail to:
Rickeys Hyatt House Hotel
4219 El Camino Real
Palo Alto, CA 94306
telephone: (415) 493-8000

Or call (800) 228-9000. Mention this conference for the special rates shown here.

Design Languages: A brief discussion highlighting the major features of CDL, DDL, ISP, PMS and AHPL.
System Level Description: The Logos and SARA systems.
Register-Transfer-Level Simulation: A Brief Description of Current Techniques.

Schedule:
8:00 a.m. - 9:00 a.m.  Late registration
9:00 a.m. - 5:00 p.m. Lectures
Lecturer: Prof. W. M. van Cleeuwpunt, Digital Systems Laboratory, Stanford University

REGISTRATION
5th Annual Symposium on Computer Architecture

CONFERENCE REGISTRATION

Members Non-members Full-time Students

On or before March 10, 1978 □ $75 □ $85 □ $15
After March 10, 1978 □ $85 □ $95 □ $20

TUTORIAL REGISTRATION

Members Non-members

On or before March 10, 1978 □ $55 □ $65
After March 10, 1978 □ $65 □ $75

Check if you need transportation information □

Name ____________________________
Affiliation ________________________
Address __________________________

ACCOMMODATIONS
Conference Name: Fifth Annual Symposium on Computer Architecture, April 3-5, 1978

NAME OF GUEST ARRIVAL DATE DEPARTURE DATE

NAME AND ADDRESS # ROOMS # PEOPLE

single ( ) $32.00
double ( ) $38.00
twin ( ) $38.00
triple ( ) $44.00
quad ( ) $44.00

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