The prospect of a special issue on semiconductor memories might very well evoke an initial reader response that falls somewhere short of fervent. After all, isn’t the subject amply treated in the trade and professional press? Product announcements and advertisements of new devices abound. What more can be said on the subject?

Before I try to answer that question, consider for a moment the recent history of semiconductor memory development. As L.C. Hobbs so aptly observed in his guest editor’s introduction in the December 1976 issue of Computer, “we have almost always overestimated what will be accomplished in the short term, and underestimated what will be accomplished in the long term.” The implications of that observation are great—and they have probably never been more apparent than they are today.

In the last decade, a startling increase in the complexity of silicon integrated circuit chips has occurred, primarily in the areas of memory and microprocessor modules. Much of the increase was expected, but the initial projections generally failed to anticipate the continuing increases in complexity.

Advances in memory density have been particularly dramatic. Given fixed lithographic layout rules, over two orders of magnitude reduction in memory cell area—and consequently two orders of magnitude increase in complexity—occurred in the period between 1963 and 1970. This has shown itself in a reduction in the number of devices per cell from six devices for early 64-bit/chip designs to two equivalent devices per cell for the most recent 16K-bit/chip designs.

This has not been the only method of increasing complexity of chips, although it does represent the major portion of the increase to date. The most advanced current cells are now at a point where the cell area is within a factor of 5 of the area of an array of parallel metal lines crossing an array of parallel diffusions containing contact holes at the intersections. Thus, few if any further reductions in cell size can be expected to take place due to electrical design innovations in the basic cells.

Further advances in the future will probably occur through reductions in basic device geometry, which are in turn the result of reductions in line widths achieved by new lithographic processes. Design rules have decreased only by a 2 to 1 ratio in the period described (from 5-10 μm to 3-5 μm), providing a 4X increase in circuit density, while cell simplification has resulted in almost 16 times greater density due to a 4:1 decrease in cell complexity, leading to an overall RAM circuit density increase of 60 to 70.

The increase in complexity has taken place in almost equal time increments, each representing a quadrupling of the number of bits per chip, occurring in about two-year periods.

Extrapolating this to the future, it should be apparent that further reductions in cell area due to circuit techniques will not lead to the next quadrupling of cell complexity and that the only increase will take place by introduction of tighter design rules, using electron-beam or X-ray projection techniques.

With this added complexity, a new set of design constraints and problems have risen on the horizon to challenge (or plague) the system users. Hence this special issue of Computer.
more powerful than—the conventional computer memory elements. In a sense, serial memories of these types should be considered as new system components, rather than direct replacements for existing systems, if their full capabilities are to be exploited.

With the increased reliability expected of some systems, and with the desire of system developers to achieve a least-cost overall system, the testing of devices themselves must be considered in light of initial device cost, in-house repair, and field service. This has given rise to a wide variety of approaches to achieve this least-cost point. One approach, described in the paper by Greenwood of Reliability, Inc., involves the reliability screening of devices to reach this tradeoff. This paper presents a method in which the “reliability-at-any-cost” approach is not employed in the military/aerospace field to the throwaway approach in the calculator/pocket radio mass market.

As more and more devices are placed on a chip, the failure modes of the devices become more complex, and testing of the devices becomes a serious consideration in the production of good devices for customers, as well as evaluation of devices by the customers. The general topics of memory testing as well as the general concept of detection of pattern-sensitive faults have already been addressed in the literature. However, a new method of testing for adjacent pattern interference faults in RAM chips, discussed in the paper by Srini of Virginia Polytechnic Institute and State University, presents a minimal set of tests which may be used to detect one of the common fault modes of existing technology devices, reducing the test interval needed for LSI chips.

So, by comparison with the customary fare, these issues represent a somewhat different aspect of the semiconductor memory field. One can easily pick up the latest issues of trade magazines and view the devices advertised on their pages merely as solutions to his immediate problems. For example, recent announcements include a single microprocessor chip with internal ROM and mask-programmable memories; and first-in/first-out and associative memory chips are also available. But as suggested above and as summarized by the Vail Computer Elements Workshop report which winds up the theme papers in this issue, these devices are becoming more than just components in a system. Indeed, they can lead to radically new architectural alternatives, and they must be considered in this light in the overall task of computer system design.

Matthew Francis Slana is the supervisor of the System Design Group in the AUTOSEVOCOM II Development Laboratory, Bell Telephone Laboratories, Naperville, Illinois, where he is currently responsible for project coordination, system architecture, and requirements for a military communications switching system. His experience includes design and development of the time division network for No. 4 ESS, exploratory circuit and network development, device evaluation, transmission testing, and computer device and system research. In addition, he is a professor and head of the Electrical Engineering Department at Midwest College of Engineering, Lombard, Illinois, where he currently teaches courses in linear systems, network analysis, and network synthesis on the graduate level. He received the BSEE (with high honors) from the University of Notre Dame in 1957, the MSEE from the University of Wisconsin in 1958, and has taken course work towards the PhD at Polytechnic Institute of Brooklyn. Slana is a member of the IEEE and has been active in the Computer Elements Technical Committee of the IEEE Computer Society.