REPOSITORY

technical papers
covering the full range
of computer system design

The Repository, a collection of over 2600 technical papers and documents relating to computer science and engineering, is maintained by the Computer Society as a service to the information processing community. Some of the papers have been refereed; others have not.

If you have a paper of interest to the computer field, you are invited to submit two copies, including abstract and index terms, to the IEEE Computer Society Editor-in-Chief, 5885 Naples Plaza, Suite 301, Long Beach, CA 90803. Be sure to include a cover letter giving permission to enter the paper in the Repository. Entry in the Repository does not constitute publication.

Photocopy prices are $1.00 per page. Add $1.00 service charge to all orders under 50 pages. Microfiche copies are available for $2.50 each manuscript under 50 pages, plus $2.50 for each additional 50 pages or fraction thereof. Be sure to state the R number, listed before the author's last name, of each paper you order. All Repository items must be prepaid except for companies or institutions with established accounts. A $2.00 invoice charge will be added to all non-prepaid orders. Please make your check or money order payable to the IEEE Computer Society.

R77-1—Chroust, G., "Implementation of Expressions—A Bibliography" (23 pp., IBM Laboratory, Vienna, Austria)

This bibliography contains about 200 references concerning the implementation of arithmetic and logic expressions. It appears that most papers published before October 1971 are contained in the bibliography.

R77-2—Law, Edward K. H., "Micro-Maxi Data Transfer System" (118 pp., University of Pittsburgh, Pittsburgh, Pennsylvania)

The design project described interfaces the Intellec 8 microcomputer with the PDP-10 timesharing system, primarily to provide a mass storage device for the Intellec 8. The task included a study of the timing characteristics of the I-8 I/O and instruction execution, a study of the data transmission characteristics of the PDP-10 timesharing system, and the design of a hardware interface between the I-8 I/O port and the PDP-10 timesharing lines. The I-8 software necessary to establish a communication link between the teletype writer on the I-8 and the PDP-10 timesharing system is described, along with the necessary I-8 and PDP-10 software to control the data transfer between the systems, including the error checking capability. Finally, the potential benefits and extensions of this design are enumerated.

R77-3—Mamrad, Sandra A. and Paul D. Amer, "Workload Characterization Using Selected Pattern Recognition Techniques" (22 pp., The Ohio State University, Columbus, Ohio)

A representative test workload is required for various computer system performance evaluation activities. Statistical pattern recognition provides a surprisingly appropriate framework and tools for developing such a workload. In particular, feature extraction and selection techniques are useful for finding the best set of performance variables which characterize system resource demands, and clustering analysis techniques are appropriate for dividing jobs into subsets or classes in a manner that generates metrics for quantitatively describing the outcome of the comparison of real workload and test workload properties. A workload generation methodology based on these pattern recognition techniques is proposed and an experimental application of the methodology is presented.

R77-4—Heinzel, Werner, "Interactive Programming of Microcomputers by Using a Resident Compiler" (7 pp., Universität Bochum, Bochum, West Germany)

This paper discusses a method to program microcomputers using a high-level language. Besides the interactive compiler itself, a linkage editor for absolute addressed machine code, a library for standard functions, and command system for microcomputers are presented. The compiler design is demonstrated using the Intel 8086 microprocessor. All modules are core resident. In addition to the common microcomputer development system without disk, only a teleprinter is used for program development.


An algorithm for the minimization of ternary switching functions is described. The algorithm is based on a standard binary switching function simplification method. The operations of consensus, join, and complement join on ternary switching functions are defined. The procedure of covering is discussed in detail. Systematic methods for finding all prime implicants and a minimal-cost, static-and-dynamic-hazard-free representation for operation-hazard-free ternary switching functions are presented which are suitable for both computer and hand execution. Illustrative examples are also presented.

R77-6—Rao, C. V. Kameswara, "Fault Detection in Irredundant Combinational Networks" (28 pp., University of Linköping, Linköping, Sweden)

A procedure for deriving a complete test set covering all single faults in irredundant combinational networks is presented. Faults of the nature stuck-at-1 and stuck-at-0 in networks composed of AND, OR, NAND, NOR, and NOT gates are considered. It is possible to obtain the minimal test set covering all the faults from this complete test set.
This thesis explores two objective approaches to language design. An experimental approach to language design recognizes the human element in programming and attempts to achieve an optimal design by an empirical investigation of language constructs and design principles. A formal approach to language design recognizes the theoretical foundations of programming languages and attempts to achieve an optimal design by a specification of the properties of language constructs in order to expose weaknesses, inconsistencies, and design flaws. These approaches to language design are applied to an exploration of control constructs for interactive computing, particularly in computer-aided instruction (CAI). A control chart is designed that enables CAI answer judging and unifies selection and iteration. A static exception processing scheme is also examined. Two experiments tested these constructs and at the same time illustrated a methodology for conducting experiments on-line in a CAI environment. In the investigation, several design principles evolved. These are proposed as a partial basis for reasoning about language features in general.

In digital circuits there is typically a delay between the occurrence of a fault and the first error in the output. This delay is the error latency of the fault. The error latency is shown to be a geometrically distributed random variable for a very general class of faults in combinatorial methods. To obtain the value of the distribution parameter and thereby describe the error latency are given. A simple technique establishes a bound on the error latency for a given circuit. It is shown that there are circumstances where the mean upper-bound error latency is comparable to the mean time between faults. The implications of this for life expectancy calculations are discussed. Random test set generation and random testing are analyzed using the error latency model. It is shown that some faults require many more randomly generated attempts to find a test than would be required for the complete enumeration of all inputs.

A model is presented to facilitate the characterization of the error latency of a fault in a sequential circuit. A simple bound on the error latency of a fault may be obtained directly from the model so that the exact, but lengthy, calculation of the error latency may be avoided. Random testing of sequential circuits is analyzed using the error latency model. For a desired quality of test, the necessary length of the random test may be specified. Previous results on the topic of random testing are found to be valid only for a restricted set of faults.

The correspondence between Boolean network probabilities and the design formalisms of Ledley and Aiden is demonstrated.

Two experiments are conducted on-line to determine the effect of the test set on the latency of detection of a fault. The analysis of the results shows that the test set generation algorithm has a significant effect on the latency of detection of a fault. The analysis of the results also shows that the test set generation algorithm has a significant effect on the latency of detection of a fault.

Random testing and random test set generation are analyzed using the circuit error latency model. It is shown that random testing can be quite effective in testing combinatorial circuits, yet the analysis required to verify this effectiveness for a given circuit is computationally prohibitive. Random testing is an useful method of testing only if the test confidence need not be accurately verified.

A solution is given to the linear discrimination problem for more than two statistical classes, using a Generalized Fisher Criterion as distance measure. Essentially, we find the direction X on which the projections of k=2 statistical hypotheses make the Generalized Fisher Criterion maximum. Since the latter depends mainly on the minimum pairwise projected mean difference, the optimal projection direction X maximizes the worst distance. With the use of linear manifold subspaces and decomposition of the optimization problem into a union of simple convex subspaces, a closed form solution for the optimal X is obtained, and no numerical optimization techniques are needed. Such numerical optimization algorithms in high dimensional spaces were required in previously proposed methods. Using the same distance measure and similar methodology, we also derive the best discriminant vectors.

The “trace” of a rectangular matrix is defined as the trace of a square matrix obtained by appending null rows or columns at the bottom (or right) end. The problem of maximizing the trace of a matrix, by permutations and mergers of rows and columns with constraints on the resulting size of the matrix, is of interest in comparison of maps, image change detection, and registration. This paper presents an algorithm based on dynamic programming for efficient maximization of trace.
R77-17—Crane, Ronald C., “Asynchronous Serial Interface for Connecting a PDP-11 to the ARPANET (BBN-1822)” (49 pp., Stanford University, Stanford, California)

This report describes an interface to permit the connection of any PDP-11 to either the Packet radio network or the ARPANet. The interface connects to an IMP on one side, meeting the specifications published in BBN report number 1822, and to a 16-bit parallel interface (DRV-11 or DRV-11c) as described in the DEC peripherals and interfacing handbook. The interface card itself is a double height board (5.2” x 8.5”) which can be plugged into any peripheral slot in a PDP-11 backplane. The interface card is connected to the parallel interface card via two cables with Berg 40 pin-connectors (DEC H-856) and an IMP via an Amphenol bayonet connector (48-10R-18-315). All three cables and connectors are supplied with the I/O interface card. The parallel interface card (DEC DRV11-C or DRV-11) together with the special I/O interface card described in this report comprise the 1822 interface. The report includes descriptions of the operation of circuits, programming, and diagnostics for the 1822 interface.


In this study, available means of providing computer output to the blind were reviewed and criteria were set forth against which the effectiveness of a means of presentation could be measured. Available techniques were tested, and it was determined that a better method should be designed. As the result of this study, a talking computer terminal was constructed. The terminal is a computer independent, asynchronous, ASCII dial-up device and can be connected to any computer allowing this type of communication. The hardware for the terminal consists of a speech synthesis device, a microprocessor, a keyboard, an an acoustic coupler. Software to provide the control of the speech synthesizer resides in the terminal’s microprocessor system, permitting computer independence. The talking terminal was used extensively with the University of Illinois’ PDP-10 computer and proved to be a very satisfactory means of communication between a computer system and a blind computer scientist.


The idea of distributing complex software operations over several interconnected computers is gaining impetus through microprocessors and microcomputers. Such multiprocessor structures are used in process-oriented systems above all. Some structures are being studied and pilot systems built in the Siemens research labs based on Intel’s microcomputer systems like Intellic 8/80: meshed network, simple bus systems, and redundant bus system. The three systems and their important characteristics are compared.

R77-20—Snir, Marc and Amnon B. Barak, “A Direct Approach to the Parallel Evaluation of Rational Expressions with a Small Number of Processors” (15 pp., The Hebrew University, Jerusalem, Israel)

In this paper we construct algorithms and investigate the time required for the parallel evaluation of rational expressions using a small number of processors. We define algorithms which compute a polynomial with n operations in 3n+(2p+1)+O(p) time units with p processors and a general rational expression with n operations in 5n+(2p+3)+O(p) time units. These algorithms are suitable for implementation on computers with restricted data access.

R77-21—Smith, James E., “On Necessary and Sufficient Conditions for Multiple Fault Undetectability” (10 pp., University of Wisconsin, Madison, Wisconsin)

This correspondence states necessary and sufficient conditions for a multiple stuck-at fault in a combinational network to be undetected by a test set. The conditions are given in terms of fault masking relationships. It is shown that several other statements on this subject which have appeared in the literature are invalid.


Cardalert is a portable, battery-operated real-time heart-beat processor and alarm system for high-risk cardiac patients. Electrocardiograms taken from Lead II skin electrodes are converted into 8-bit digital data sequences. Digital differentiation is performed on the data, and a feature-extraction approach is utilized to locate the Q, R, and S peaks. Comparison between the present RR-interval and a running average of the previous four normal RR-intervals is performed. Wide QRS durations are also noted. A conclusion is then derived from these parameters regarding the number and frequency of premature ventricular contraction (PVC) occurrences. When a presettable criterion is met, an alarm is sent out to warn the patient of possible ventricular fibrillation. ECG tape analysis at 60 times real-time speed is possible by simply connecting the machine to an adaptor. Several arrhythmias are also recognized by the machine.

Order by R-Number. Use the Repository order form on page 86.