ON May 19-21, the Computer Packaging Committee of the IEEE Computer Society held its biennial workshop at Split Rock Lodge in the Poconos. Following the same format as in the past, the meeting featured a keynote speech and five technical sessions. Some 60 people from 14 states plus England and Japan were in attendance.

Keynote speaker Gordon Scarrott of ICL spoke on the progress made in the computer field in the last 25 years and expectations of what might happen in the next 25. Basing his talk in part on an earlier presentation at the colloquium on the stored-program computer held at the Royal Society in London, Scarrott posed the question of how long it will be economical to separate storage from processing in computer design. It is, he observed, easy to understand how this separation was derived from past limitations of technology—i.e., a core memory is a different kind of device from gate switches. But this is no longer so, and there are benefits to be derived from mixtures.

Two of Scarrott’s predictions were of specific relevance to computer packaging:

(1) Increased use of standardized units which achieve high processing power by multiple building block assembly seems to offer reduced design time and much greater utilization and interchangeability across different design lines.

(2) Groups of modules will be dedicated to serve as semi-autonomous units to do various chores in information processing.

The subsequent technical sessions covered a variety of topics, ranging from the level of chip packaging and on-board interconnections to the partitioning trends and the various strategies for optimization of a field-replaceable unit.

One of the most interesting presentations was that of Jacob Martin of MIT-Draper Laboratories, who spoke on computers in aircraft flight control. The concept of fault-tolerant computers has been evolving for some time but has certainly increased in importance with the commitment to build an on-board fault-tolerant computer for commercial aircraft flight control. It is quite evident that when a computer is considered an integral part of an aircraft flight system, and that wing areas can therefore be reduced by 20 to 30% and their structural strength greatly decreased on the assumption of nearly perfectly coordinated turns and flight maneuvers, society will have made a commitment to fault-tolerant computing involving millions of people’s lives. The redundancy of electronics that calls for “triads” followed by “voting” circuits to take out of action any off-functioning unit has been extended to multiple-loop bussing and multiple-contact connectors. It was interesting to note that the approach still seems to be conventional in terms of hardwiring, but will likely be strongly affected by utilization of fiber optic techniques for unit interconnection.

J. Kolling of Sperry Univac, St. Paul, Minn., discussed just that—i.e., the improvement in reliability and reduction in weight and size as one replaces multiple hard wires with multiplexed IF-Coax data busses and then with fiber optics “cables.” For one large computer center building, that saving in copper alone was on the order of 50 tons, and of course there were great savings in space as well.

The interface concept is for small hybrid circuits to be built into the body of the mating connectors so that the fiber optic cables could be plugged and unplugged with conventional electroconnectors at the ends.

Small hybrid subassemblies are also very much a part of the shift to electronic controls by the automotive industry. Frank Steinh of the Delco Division of General Motors discussed the design of voltage regulator and ignition control systems. He indicated some of the approaches that are being used by Delco and by others. For units whose production rate already approximates 25,000 a day, reliability problems have to be a major consideration. The very significant point of this talk was that Delco found insufficient additional reliability from the use of hermetic seals and therefore chose open-cased chip designs with a silicone jelly surface protection. Such circuits, which are not hermetically sealed and in fact are penetrated by the various contaminants of the automobile engine compartment, are found to have very high reliability even in the presence of automobile gasoline and oil fumes, nitric oxide, sulfur dioxide, high temperature, and high humidity. The reliability of automobile ignition control is also satisfactory even in very high ozone concentrations inside the distributor cap. Delco’s favorable experience with just jelly for protection is a strong argument for increasing use of such silicone materials in computer memories and central processors.

Three papers were addressed to very recent developments in the fabrication of the printed circuit card or field-replaceable unit. Jeff Waxweller of Algorex gave a review on the
trends in the design of field replaceable units. Waxweiler, who works with larger boards and multichip packaging, pointed out that a number of his boards are ceramic with up to ten co-fired metal layers. In general, his ceramic assemblies had the chips bonded on by epoxy bonding and wire bond leads. I/O points on some of the designs are brought through to the backside for testing.

Honeywell (Phoenix) also uses ceramic-square packages of 80 leads with the leads on 50-mil centers. Such packages, 2½ to 3½ inches square, are used as a substrate for the individual LSI or MSI chips which are connected by tape automated bonding. The company has made a deliberate choice not to go all LSI because that would give too many chip types. Instead, with a self-imposed limitation to try to achieve less than 50 chip types, Honeywell uses a mixture of MSI and LSI chips.

In a similar paper by Chiba of Hitachi, the logic LSI’s for the HITAC M-170 and M-180 computers were described. The Chiba paper was noteworthy because of its exploration of the relationship between the delay time and the effective packing density. From his graphic plots he established that minimum power density occurs when the circuit delay is one-third of the system delay or, putting it another way, when the packaging delay is no more than twice the circuit delay. Since the packaging delay is inversely proportional to the square root of the effective packing density of gates, one can derive an indication of the optimum packing density that one should strive to achieve.

In the discussion of these strategies for the field-replaceable unit, much data was brought forth to indicate the changes in packing density, pin-outs, gate per board, and wattage dissipations for such plug-in boards. Leading this portion of the program was Don Franck of IBM, who proposed a number of useful charts to demonstrate or display the trends in circuit pin and packing density over the years. The ensuing discussion proved to be of such general interest that it was felt that the Computer Packaging Committee should take the initiative in gathering information from a large segment of the computer industry and producing a set of charts based on that reporting. Since all the charts to be produced are based on the characteristics of the field-replaceable unit as actually shipped in production systems in a particular year, the information cannot be construed to be private or proprietary, but it was still felt that the points on the curves should not be readily identifiable as to manufacturer. A subcommittee of the Computer Packaging Committee was established with instructions to produce the required questionnaire and gather the information.

In addition to system interconnection and board interconnection areas of seminar presentation, there was also a review of current trends in interconnection from the chip to the printed circuit board or first-level package.

After a review of wire bonding, beam lead bonding, chip flip bonding, and tape automated bonding, there was a discussion of the need for a standard LSI package of lead or pin counts ranging from 25 to 100. Dan Amey of Sperry Univac has taken the lead in producing recommendations for such a standard package, with the expectation that such a standard would make possible a line of sockets and connectors, plastic and ceramic chip carriers, and the associated manufacturing tooling. This possibility, which had been previously discussed at the Drexel Microcircuits Conference in February and the Computer Packaging Meeting in March, has led to an active program aimed at producing a standardization document for circulation by the JC11 JEDEC Committee of the Electronic Industry Association in early fall. The implications of this proposed standard are beyond the scope of this conference report, but will be thoroughly discussed and presented at conferences such as the Semiconductor Test Symposium, NEPCON West and East, and possibly the Electronics Components Conference in the spring.

This workshop, the major informal non-proceedings conference of the Computer Packaging Committee, is held every other year at Split Rock. Bi-monthly meetings are held in New York at the United Engineering Building the third week of the odd-numbered months and are normally attended by those members within a 600-1000 mile radius of New York. In addition to these informal technical meetings and workshops, the Computer Packaging Committee also sponsors technical sessions at major packaging conferences such as NEPCON and the Electronic Insulation Conference, and arranges sponsored company tours. These other meetings provide the opportunity for some regional contact with the Packaging Committee for those too far away from New York to attend the regular bi-monthly meetings.