R75-303—Takiyama, R., "Signal Classification by Two Threshold Elements with Analog Inputs" (19 pp., Department of Visual Communication Design, Institute of Design, Fukuoka, Japan)

The threshold element with analog inputs is one of the fundamental elements, which realizes a linear discriminant function. Although this is useful for synthesizing signal classification systems, there is a limit in ability of the linear separation. To improve this, signal classification systems which are synthesized by two threshold elements (two threshold elements network, TTEN) are investigated. Signals which are correctly classified by a TTEN are called 2-separable. The functional properties of the TTEN are clarified and a necessary and sufficient condition for signals to be 2-separable is shown. Under the condition, an iterative procedure to obtain the parameters, which characterize the TTEN correctly classifying the signals, is proposed. A learning procedure to obtain the parameters is also proposed. The effectiveness of both procedures is shown experimentally.

R75-304—Namandra, P. M. and K. Fukunaga, "A Branch and Bound Algorithm for Feature Subset Selection" (28 pp., School of Electrical Engineering, Purdue University, Lafayette, Indiana)

A new optional feature subset selection algorithm based on branch and bound techniques is developed to select the best subset of m features from a set of n features. Existing procedures for feature subset selection, such as sequential selection and dynamic programming, do not guarantee optimality of the selected feature subset. Exhaustive search, on the other hand, is generally computationally unfeasible. The present algorithm is very efficient, and selects the best subset without exhaustive search. The algorithm is applicable to a broad class of criteria. Computational aspects of the algorithm are discussed. Results of several computer experiments are presented; they demonstrate the very substantial computational savings realized.

R75-305—Chang, D., D. Lueck, and D. Lawrie, "On the Effective Bandwidth of Parallel Memories" (35 pp., Department of Computer Science, University of Illinois, Urbana, Illinois)

The object of this paper has been to bring together several models of interleaved memory systems and to expose some of the underlying assumptions about the address streams in each model. We derive the performance for each model, either analytically or by simulation, and discuss why it yields better or worse performance than other models (e.g., because of dependencies in the address stream, hardware queues, etc.). We also show that the performance of a properly designed system can be a linear rather than a square root function of the size.

R75-306—Christensen, R., "Contrived Patterns, Trying to Avoid Them without Trying Too Hard" (25 pp., Biotechnology Program, Carnegie Mellon University, Pittsburgh, Pennsylvania)

The problem of contrivedness in clustering algorithms for pattern discovery is discussed. A method is described for computing the entropy of chance correlations for a cluster in feature space as a function of the feature space dimension and the dimensionality of the subspace defining the cluster. This permits one to measure the difference between the conditional classification entropy on a training sample for a partition of feature space and the entropy of chance correlations for the partition. Both theoretical considerations and actual computer runs yield a chance correlation entropy curve as a function of cluster dimensionality with a dip at a particular (data dependent) number of features. The chance correlation classifying ability of the pattern discovery algorithm is greatest for clusters of this dimensionality.

R75-307—Stockman, G., "A Transformation for the Detection of Symmetry in a Set of Picture Points" (20 pp., L.N.K. Corporation, Silver Spring, Maryland)

A transform is discussed which can be used to detect symmetrical sets of points in digital pictures. The transform is logically quite simple, but care must be taken to reduce computational steps in a sequential software implementation. Several examples are given to illustrate its use.

R75-308—Cao, V., and R. J. Smith, II, "Construction of Steiner Trees Using the Method of Variable Shortest Connecting Networks" (40 pp., Lawrence Livermore Laboratory, University of California, Livermore, California)

This paper describes a technique for the determination of minimum or near-minimum length Steiner trees in an obstacle-free rectilinear environment. A compact notation is used to describe the procedure, and several examples illustrate its use.
R75-309—Elshoff, J. L., “An Analysis of Commercial PL/1 Programs” (31 pp., Computer Science Department, Research Laboratory, General Motors Technical Center, Warren, Michigan)

The source code for 120 PL/1 programs from several General Motors commercial computing installations has been collected. The programs have been scanned both manually and automatically. Some data from the scanning process is presented and interpreted. The programs are considered with respect to five attributes, (1) the size of the programs, (2) the readability of the programs, (3) the complexity of the programs, (4) the discipline followed by the programmers, and (5) the use of the programming language. Each area is reviewed with pertinent data presented whenever it is available. Although the programs analyzed are written in PL/1, persons from installations using other languages, particularly COBOL, have indicated that the information presented is typical.


With the recent advances in LSI microprocessors and the increasing sophistication of minicomputers, multiprocessor systems are certain to attract more attention. Developmental systems have been built at Carnegie-Mellon University (C.mmp), and at Bell, BBNake, and Newman (PLURIBUS IMP). Moreover, some of the issues in programming multiprocessors are better understood. Analytic and simulation models of memory interference have been reported in the literature. These models provide tools for analyzing various system architecture alternatives. Some of the design parameters are processor speed, memory speed, number of processors, number of memories, use of cache memories, high order versus lower order interleveling, and memory allocation. This paper applies existing analytic and simulation models to the multiprocessor design space and presents guidelines for the multiprocessor system architect. Preferred design alternatives and tradeoffs are outlined.

R75-311—Clifton, M. H., “Randell's Method and Dynamic Storage Allocation Systems” (76 pp., Technical Report UIUCDCS-R-75-734, Department of Computer Science, University of Illinois, Urbana, Illinois)

This report is concerned with the effective use of main computer storage by dynamic storage allocation systems. A number of dynamic storage allocation methods are described. Simulation experiments provide results of storage utilization for each method. These results are used to compare the effectiveness of the methods in allocating storage for varying parameters.


The following interactive diagnostic system can be devised to analyze synax errors detected in an interactive time-sharing compiler. The internal system is “automatic,” that is, it is driven by the compiler’s parser tables. The error system behaves like a consultant by suggesting “possible corrections” of the program to the user, and at any time the user can proceed to fix the program or request further suggestions. In addition, the “possible correction” diagnostic suggestions can refer to not only individual “tokens” in the user’s program, but also higher-level constructs, such as “expressions,” “array bounds,” etc.

R75-313—Tindall, M. H., “An Interactive Table-Driven Parser System” (87 pp., Technical Report UIUCDCS-R-75-745, Department of Computer Science, University of Illinois, Urbana, Illinois)

The design and implementation of the parser system for a multi-lingual compiler on the PLATO IV computer-aided instructional system is described. A brief discussion of the formal transition diagram parsing method is followed by a description of the assembler language used to specify the syntax of a programming language and the description of the actual parser tables.


This thesis presents a general computational method, amenable for an efficient implementation in digital computing systems. The method provides a unique, simple and fast algorithm for the computation of many complex mathematical functions, such as the evaluation of polynomials, rational functions, and arithmetic expressions, solving a class of systems of linear equations, or performing the basic arithmetics. In particular, the method is well-suited for the fast evaluation of commonly used mathematical functions. The method consists of (1) a correspondence rule which reduces a given computational problem f into a system of linear equations L and, hence, to the problem f in O(m) addition steps with an m-digit precision. However, the time to execute each addition step is independent of the operand precision. The algorithm is deterministic and always generates the result in a digit-by-digit fashion, the most significant digit appearing first. Therefore, the algorithm provides for an overlap in a sequence of computations as well as for a variable precision operation. The method, in general, has favorable error properties and simple implementation requirements.

R75-315—Halbur, J. D., “A Code Generator for the CLEOPATRA Language” (57 pp., Technical Report UIUCDCS-R-75-739, Department of Computer Science, University of Illinois, Urbana, Illinois)

CLEOPATRA is a systems implementation programming language. A compiler for the CLEOPATRA language has been divided into two parts—the analysis phase and the code generation phase. These two parts communicate by means of an intermediate text and symbol table. This report describes the design of the code generator which consists of storage allocation, expression evaluation, and statement translation. The intermediate text is also described. The code generator program is written in PL/1 and generates code for the IBM 360. A subset of CLEOPATRA has been implemented, because this compiler is intended as a bootstrap for future compilers.

R75-316—Ranshaw, J. W., “ROBOCAR: Educating the Layman in Computer Science” (47 pp., Technical Report UIUCDCS-R-75-741, Department of Computer Science, University of Illinois, Urbana, Illinois)

ROBOCAR is a series of lessons on the PLATO IV System designed to teach computer programming in an environment which allows fundamental concepts of programming to be illustrated in an intuitive setting and promotes interactive practice through the use of animated graphics controlled by a text-editor and interpreter.


High-speed computer systems usually organize their storage into several modules. Each module can operate simultaneously. Hence, several modules can be accessed at the same time. This effectively increases the throughput, and the computational speed of the system. In this report, we first describe several interleaved memory models designed and analyzed by other people. We report their results and also show some further improvements. We then present our new models and derive appropriate performance figures. The difference between previous models and our new models is the way we handle the requests and conflicts. Some of the circuit design problems are also discussed briefly in this report.


In the first part of this thesis, the architectural development of a specific microprocessor machine is presented. The experiences gained during this design project indicate that there is a “best” system architecture for a given problem. Design options become available only on lower design levels, mainly in control units. The second part of the paper analyzes the choice between microprogrammed and hardwired realizations of control units. A model which predicts the costs of equivalent microprogrammed and
hardwired control units is developed. This model predicts that the cost of a hardwired control unit will increase faster than that of its microprogrammed counterpart, the control signals which must be emitted become more complex. From the same foundations, a model for the reliability of both methods can be obtained. This model predicts that the availability of a microprogrammed control is nearly independent of the control sequence. Hardwired control units, however, suffer from decreased reliability as control complexity grows.

R75-319—Chung, W. L., “Automatic Curve Fitting for Interactive Display” (96 pp., Technical Report UIUCDCS-R-75-713, Department of Computer Science, University of Illinois, Urbana, Illinois)

This thesis presents a simple, economical, and reliable algorithm for calculating cubic polynomials with continuous slopes and curvature which are used to display curves on the screen of CRT-like graphics terminals. An adaptive local scheme is based on interpolating piecewise cubic polynomials and calculating an error measure for each point. The system accepts a large number of data points as they are generated one point by one by an ordinary differential equations package and compresses the data into a compact picture representation. The important features of this algorithm can be found in its adaptive use of two quantitative measures of approximation—a local least-squares error norm and a pseudo distance norm, and its ability to regenerate aesthetically pleasing curves using the piecewise cubic polynomial interpolants with relatively few knots by one-sided, local computational procedures. The advantages of one-sided, local procedures are the economical computation based on local data and the fast search for knots.

The problem of numerical stability imposed by one-sided, local procedures is solved by the idea of extended intervals which were intuitively developed and proved to have interesting mathematical and computational effects on the stability and error behavior of the algorithm. The scheme can be used for compression, transmission, and display of graphical data in both on-line and off-line environments.


The multiprocess, multiuser EXEC provides coordination and control for EUREKA, an experimental information retrieval system. The EXEC is a framework on which the constantly changing hardware and software of EUREKA are attached. It is intended to isolate modules from each other and formalize interactions between modules. To this end the EXEC provides process control, address space management, synchronization primitives, and I/O control. Whenever possible, it takes advantage of its knowledge of the state of the system to overlap execution and waiting phases of various modules. In an analogous manner it overlaps the operation of several users to more fully utilize the hardware and software resources of the system.

R75-321—Kovacs, G. L., “Some Experiments on the Placement Problem” (49 pp., Computer and Automation Institute, Hungarian Academy of Sciences, Budapest, Hungary)

One of the most crucial parts of computer-aided design of computers and other electronic equipment is the placement of elements. The optimal placement of elements (IC, MSL, etc.) on printed circuit boards or the placement of the printed circuit boards in larger units (e.g., racks) is of great importance because a "not good" placement may obstruct the effectiveness and usefulness of the final wiring methods. On the other hand, because of the complexity and size of practical problems, there is no method to guarantee an optimal placement. That is why several heuristic algorithms were developed to find "good" placements. In our paper constructive initial-placement, iterative placement-improvement, and combined methods are investigated, examining results of these kind of programs through some real problems. We are trying to find some basic characteristics of the placement problem by means of experiments of the effects of simplifications which are necessary to speed up computation (e.g., complete graph lengths versus minimum length tree, Manhattan distance versus Euclidean distance, and the assumption of all elements to be points, etc.).


This PLW language and information helpful in using the present PLW compiler is detailed. The PLW language is in many respects like PL/I. The object language of the compiler is FORTRAN. Hence the compiled code is, to a great extent, portable.

R75-323—Montanelli, R. G., Jr., "CS 103 PLATO Experiment, Fall 1974" (31 pp., Technical Report UIUCDCS-R-75-746, Department of Computer Science, University of Illinois, Urbana, Illinois)

In order to determine the effectiveness of replacing a lecture on FORTRAN with PLATO CAI material in an introductory computer programming class, an experiment was conducted. The students in CS 103 were randomly divided into two groups, with students in the PLATO (P) group getting a PLATO lesson in place of one of the two weekly lectures throughout the semester. Results indicated that there were no significant differences between the groups on any objective test and that the students in the P group were initially happy and satisfied with the PLATO materials, although there were a few complaints by the semester's end. These problems have been fixed, and PLATO should be able to routinely substitute for one lecture a week in introductory computer programming courses.


A method to machine grade student-generated structured programs is described. This method (Semantic Formulation Method, SFM) is compared and contrasted with two other methods of grading programs: the test data (testing the program by inputting data) and the deductive examination methods. It is shown that the SFM is ideally suited for grading programs in a computer-based education environment. A computer program implementing the SFM on the PLATO IV Computer-Based Education System is described. The class of structured programs utilized in the PLATO IV implementation version is smooth flowcharts. Smooth flowcharts are a subset of flowcharts which only allow the DOWHILE and IFTHENELSE in their control structure. The SFM of grading structured programs is based on the artificial intelligence paradigm of "description, representation, and deduction." The special purpose deduction scheme is tailored to prove in an efficient manner that two structured programs (the student's and the instructor's) are equivalent.

R75-325—Bhat, K. V. S., and Bharat Kinarwala, "An Algorithm for ncn Optimum Assignment Problem" (18 pp., Department of Electrical Engineering, University of Hawaii, Honolulu, Hawaii)

In this paper we present an algorithm for finding an optimum assignment for a n by cn matrix M in n iterations. The method uses systematic permutations on the rows of M and is based on the properties of optimum assignments. The implementation presented in the paper requires time at most O(cn) and memory n2+c into locations for solving a dense n by cn problem.
R75-326—Kunarwala, Bharat, and K. V. S. Bhat, "Theory of Output Set Assignments and Degree Switching Operations" (25 pp., Department of Electrical Engineering, University of Hawaii, Honolulu, Hawaii)

In this paper we study the basic aspects of the output set assignment problem using graph theory. The output sets of a n x n matrix A constitute a set of disjoint cycles of total length n in the network (i.e., a graph having weighted directed edges including self loops) of matrix A. We introduce two new graphical transformations viz., the degree switching operations (DSO) in a network and study their properties. The DSO yield output sets and lead to all graphs that can be associated with a given matrix A. Possible applications for the theory are indicated.

R75-327—Bhat, K. V. S., and Bharat Kunarwala, "An Efficient Algorithm for Output Set Assignment in Large Scale Systems" (21 pp., Department of Electrical Engineering, University of Hawaii, Honolulu, Hawaii)

In this paper we present an efficient algorithm for finding an output set for a given sparse n x n nonsingular matrix A based on the combinatorial properties of output sets and the newly defined pseudo-degree of switching operations on networks (or graphs having directed weighted edges including self loops). An implementation of our algorithm uses efficient search process using cycle seeking strategy (CSS). The computational complexity of our algorithm is given. The computational properties of our algorithm has been compared with three other algorithms using randomly generated test matrices.

R75-328—Hahner, E. C. R., "Addressable Units of Program and Data" (8 pp., Computer Science, University of Toronto, Toronto, Canada)

Factors influencing the choice of the addressable unit of main memory in computer designs are discussed. A rational basis for choosing the addressable unit of program and data is suggested.


Technological advances have made possible the development of advanced hybrid computing systems (AHCS) with cost and speed advantages of at least 30:1 over pure digital systems for solving dynamic problems. Benefits from such systems are important in improving the effectiveness of research and many fields and, when used as a complement to today's pure digital computer systems, in allowing more flexibility at less expense. This proceedings contains 27 papers examining various aspects of AHCS.


In the February 1967 issue of IEEE Transactions on Computers, Gimpel presents an algorithm for finding the TANT networks with the minimum number of gates for a given switching function. The algorithm involves the formation and solution of a cover and closure table (CC-table) which are major bottlenecks in computer processing of the algorithm. This paper presents several alternative methods for solving the CC-table in Gimpel's algorithm, which are suitable for computer processing. It also presents the results of implementing these methods into computer programs and using them to find the TANT networks with the minimum number of gates for some randomly selected switching functions.

R75-331—Danielson, R. L., "PATTIE: An Automated Tutor for Top-Down Programming" (114 pp., Technical Report UIUCDCS-R-75-753, Department of Computer Science, University of Illinois, Urbana, Illinois)

The Department of Computer Science at the University of Illinois has undertaken a project to automate a substantial portion of its introductory computer science courses on the PLATO computer-assisted-instruction (CAI) system. Experience with teaching programming skills has indicated the importance of teaching beginning students how to develop a program, as well as specific programming languages. This thesis describes a CAI tutor for top-down programming which provides a detailed example of the stepwise refinement process. The tutor guides the student to a solution of a specific problem by judging the correctness of suggested refinements input by the student in natural language. An AND-OR graph is used as the model of top-down programming process. Techniques used in the tutor are sufficiently general that the design may be used for tutors in other subject areas.

R75-332—Koch, H. S., "Concurrency in Real-Time Information Systems" (28 pp., Department of Computer and Information Science, The Ohio State University, Columbus, Ohio)

In many systems, concurrent processes that do not change variables common to them do not have to synchronize their activities. It is shown that some disjoint processes must be synchronized in real-time information systems. Two requirements of many real-time information systems are that if a query Q is submitted at time T, all queries submitted before T are not affected by (non-interference requirement) and all queries submitted after T are affected by Q (influence requirement). It is shown that because of these two requirements certain disjoint and non-disjoint processes must be synchronized. Proofs are supplied that identify which processes cannot be run concurrently, no matter which synchronization method is used. Formulas are then developed to calculate which processes can be concurrently executed. This leads to the development of design program for the system designer model a system that can have many processes overlap execution.

R75-333—Cutter, J. R. and David Fieske, "A Stochastic Control System" (15 pp., Technical Report UIUCDCS-R-75-752, Department of Computer Science, University of Illinois, Urbana, Illinois)

This paper is concerned with a control system that uses stochastic techniques as the means to reach the steady-state point. The main part of the system is a temperature transducer which outputs a stochastic sequence. The time average of the stochastic sequence is dependent upon the temperature. This sequence is then used to control a heater. A description of this system is included in this paper as well as the appropriate theory and results. A system was also constructed.

R75-334—Liu, P. S. and F. J. Mowle, "Techniques of Program Execution with a Writable Control Memory" (40 pp., School of Electrical Engineering, Purdue University, West Lafayette, Indiana)

The objective of the present paper has been to investigate possible methods to reduce a program's execution time by detecting and converting automatically the more frequently executed program parts, mostly inner loops, into microcode. The methods proposed were static loading of inner loops, overlay of inner loops, and a user-aided scheme. Using FORTRAN programs as the test programs, a simulation...
program was written to measure the gain achieved by each method. A final gain between 1.59 and 4.76 was achieved by the proposed methods for memory speed ratios between 3 and 8. It was found that 90% of the individual final gain of the test programs could be obtained with writable control store requirements that were less than 40% of the final requirement of each program. Effects of some software techniques and special hardware features are also presented.

R75-335—Sato, Hiroshi, "An Outer Bound to the Capacity Region of Broadcast Channels" (41 pp., Technical Report B75-21, The ALOHA System, University of Hawaii, Honolulu, Hawaii)

An outer bound to the capacity region of broadcast channels is derived by using the mutual information between an input ensemble and a joint output ensemble when only separate messages are allowed to be sent between each source-user pair. We first introduce a region which is proved to be an outer bound by making use of the above mutual information calculated from the joint conditional probability. Then we obtain the final outer bound by taking the intersections of these regions over all joint conditional probabilities that have the same marginal conditional probabilities. For the degraded broadcast channel, the first region is the intersection of all regions. Common messages between the two users are also discussed.

R75-336—Sriiri, V. P., "Fault Diagnosis of Microprocessor Systems" (20 pp., Department of Mathematics, Virginia Polytechnic Institute and State University, Blacksburg, Virginia)

The logical, stuck-at-type faults that cause the incorrect operation of the microprocessor (LSI processor) in a microprocessor system are detected by using the instructions of the processor after providing a "reliability measure" to the instructions. The RAM memory and other parts of the system are tested by programs executed on the microprocessor. The test programs are divided into two categories: resident diagnostic programs for detecting faults and non-resident diagnostic programs for locating faults to LSI chips in the system. The programs are executed under the control of a diagnostic supervisor.

R75-337—Chow, C. K., "Determination of Cache's Capacity and its Matching Storage Hierarchy" (24 pp., IBM Thomas J. Watson Research Center, Yorktown Heights, New York)

The optimum capacity of a cache memory with given access time is determined analytically based upon a model of linear storage hierarchies wherein both the hit ratio function and the device technology-cost function are assumed to be power functions. Explicit formulas for the capacities and access times of the storage levels in the matching hierarchy of required capacity and allowable cost are derived. The optimal number of storage levels in a hierarchy is shown to increase linearly with the logarithm of the ratio of the required hierarchy capacity and the cache capacity.


This paper deals with an anomalous behavior of input synchronizers which results in random errors of any asynchronously interfaced synchronous digital system. These errors are caused by an indefinite response time to the flip-flop recovering from a metastable state. Their probability is derived from the analysis of the timing diagram and the measured probability distribution of the anomalous response times. The mean expected response time of the SN747174, for example, is estimated upon the statistical measurements of a set of flip-flops. The presented measurement technique is usable for any type of input synchronizer. Two usual ways of reducing the probability of failure are illustrated by means of results obtained upon measurements of the SN747174. Two possible fundamental solutions of the metastable state problem in the clocked systems are described.

R75-339—Izquierdo, F. J., "A Generator/Grader of Problems about Syntax of Programming Languages to Be Used in an Automated Exercise System" (23 pp., Technical Report UIUCCS-R-75-7, Department of Computer Science, University of Urbana, Illinois, Illinois)

The approach to generate problems about errors in the syntax of programming languages is presented. The three most described are instructor writing problem specifications, student working on a problem, and student reviewing a problem.

R75-340—Bagley, J. D., "Microprogrammable Virtual Machines" (16 pp., Computer Science Department, IBM Thomas J. Watson Research Center, Yorktown Heights, New York)

The introduction of computers which have user alterable microprograms presents users with flexibility and a problem. To take full advantage of the opportunity to tailor the architecture of the computer to the application domain, the problem of microprogram development and testing must be solved. The techniques outlined here provide a tool which furnishes the microprogrammer with a virtual machine which is microprogrammable. The function provided is similar to that provided by a simulator, but the technique is presented and allows multiple microprograms to be executed concurrently with regular programs on a single real machine.

R75-341—Chen, S. C. and D. J. Kuck, "Combinational Circuit Synthesis with Time and Component Bounds" (45 pp., Department of Computer Science, University of Illinois, Urbana, Illinois)

New results are given concerning the design of combinational logic circuits. We give time and component bounds for combinational circuits specified in several ways. For any sequential machine defined by linear recurrence relations, we discuss an algorithm for the synthesis of equivalent combinational logic. The procedure includes upper bounds on the time and components involved. We also discuss the transformation of nonlinear recurrences into combinational circuits. Examples are given using gates as well as ICs as components. These include binary addition, multiplication, and ones' position counting. The time and component bounds our procedure yields compare favorably with traditional results.

R75-342—Szollosi, Tom and A. B. Baskin, "LISP: A CAI Implementation" (44 pp., Technical Report UIUCCS-R-75-749, Department of Computer Science, University of Illinois, Urbana, Illinois)

This paper outlines the structure of a student oriented implementation of LISP on the PLATO I system. The basic design criteria and the form of the diagnostic compiler and execution interpreter are presented. The PLATO implementation affords a high level of diagnostic advice for the student of LISP. Examples of compilation and execution diagnostic messages are presented as well as a typical sample student interaction.

R75-343—Murthy, Parimi, "Carrier Sense Schemes with Hidden Terminals" (44 pp., Technical Report B-75-23, The ALOHA System, University of Hawaii, Honolulu, Hawaii)

A carrier sense scheme with random packet lengths and hidden terminals is analyzed. The system has a finite number of independent identically distributed users. The four quantities which represent the performance of the system—throughput, channel acquisition time, and recovery and failure times—are evaluated numerically. These quantities are plotted as functions of the probabilities of active and blocked users. From these basic plots the channel acquisition time vs throughput, recovery time vs throughput, and failure time vs throughput are constructed. The first two are found to be monotonically increasing while the last is monotonically decreasing. These plots are seen to vary with the average length of packets and number of hidden terminals. To understand the exact effect of these characteristics, systems with different average packet lengths are studied. Static control procedures to improve the performance are constructed. Both types of policies, based on user and channel statistics, are considered. It is seen that the policy is to be chosen based on the number of hidden terminals as well as the average packet length. The policies are aimed at optimizing throughput and channel acquisition times; they also seem to provide good recovery and failure times. It is seen that the presence of hidden terminals deteriorates the system performance.


The reservation ALOHA System with an anti-hogging mechanism is analyzed. The system has a finite number of independent identically distributed users. The performance indices of the system—throughput,
channel acquisition time, and recovery and failure times—evaluate numerically. These quantities are plotted as functions of the active and blocked user's starting probabilities. From these plots the channel acquisition time throughput, recovery time throughput, and failure time throughput curves are derived. These plots are seen to vary with average packet length and anti-hogging parameters. In all cases, the channel-acquisition vs throughput and recovery time vs throughput curves are monotonic decreasing functions, and failure time vs throughput is a monotonically decreasing function. The effect of average packet length is also studied. Static control procedures to improve the performance are then investigated. The policy varies with the average packet length and anti-hogging parameter. These are derived for optimizing throughput and channel acquisition time; they provide good recovery and failure times also. It is found that the anti-hogging parameter does not improve the performance; it merely prevents the dominance of a single user.

R75-345—Cooper, D. B. and Nael Yalabik, "On the Cost of Approximating and Recognizing a Noise Perturbed Straight Line or a Quadratic Curve Segment in the Plane" (48 pp., Technical Report NASA NSG 5036/1, Division of Engineering, Brown University, Providence, Rhode Island)

Approximation of noisy data in the plane by straight lines or ellipses or single-branch hyperbolic curve segments arises in pattern recognition, data compaction, and other problems. A number of questions concerning the efficient search for and approximation of data by such curves are examined. Recursive least-squares linear curve-fitting is used, and ellipses and hyperbolas are parameterized as quadratic functions in x and y. The error minimized by the algorithm is interpreted. CPU times for estimating parameters for fitting straight lines and quadratic curves are determined and compared. CPU time for data search is also determined for the case of straight line fitting. Quadratic curve fitting is shown to require six times as much CPU as does straight line fitting. Curves relating CPU time and fitting error are determined for straight line fitting. Lastly, results are derived on early sequential determination of whether or not the underlying curve is a straight line. A brief sketch is also provided of a formalism for incorporating noisy curve fitting in the recognition of complicated line drawings.


In this paper we analyze the throughput of an ALOHA channel when compared to that of a conventional point-to-point channel at the same power. This analysis is of interest in the case of a satellite information system employing thousands of small earth stations. For a satellite system the fundamental limitation in the downlink is the average power available in the satellite transponder rather than the peak power. Our results show that in the limit of large numbers of small earth stations the ALOHA throughput approaches 100% of the point-to-point capacity. Thus the multiple access capability and the complete connectivity (in the topological sense) of an ALOHA channel is paid no price in average throughput. Furthermore, since our results suggest the use of higher peak power in the satellite transponder (while the average power is kept constant) the small earth stations may use smaller antennas and simpler receivers and modems than would be necessary in a conventional system.

R75-347—Smith, Alan Jay, "Two Methods for the Efficient Analysis of Memory Address Trace Data" (23 pp., Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, California)

The high cost of analyzing long memory address traces has limited most researchers to short traces and analysis algorithms that are linear in the length of the trace. We suggest two methods that permit a trace to be shortened in length by one to two orders of magnitude (or more) for later further analysis. The Stack Deletion Method eliminates all references in the trace to the top k levels of the LRU stack. The Snapshot method records the reference bits of the pages in the original tape at discrete intervals and uses these bits to generate a new trace. Extensive measurements are presented, from which we conclude that there is little or no loss in accuracy using reduced traces for a wide range of memory sizes and degree of reduction.

R75-348—Wilkins, S. F. "Generation and Comparison of Equivalent Equation Sets in a General Purpose Simulation and Modeling Package" (291 pp., Technical Report UUCCDCS-R-75-709, Department of Computer Science, University of Illinois, Urbana, Illinois)

In the General Purpose Simulation and Modeling Package, the behavior of a generalized network, which is modeled graphically, is studied by analyzing numerically an equation set equivalent to the graphic model. Two methods, which operate within the same simulation environment, have been developed for generating the equation set for a network model. The equation sets generated are linear transformations of one another so that either set may be used to define the behavior of the network. One set of equations usually contains fewer unknowns, but each is more dense (i.e., contains more terms and depends on more variables). Thus it is not immediately clear which can be solved most rapidly using sparse techniques. The two methods were compared by measuring the relative efficiency of the operation of the numerical analysis programs on the two equations sets. A variety of networks were modeled and simulated using both methods to generate the data used for comparison. One method was generally found to be at least as efficient as the other method for sparsely-connected networks and markedly more efficient for densely-connected networks.


In this thesis the worst-case performance of three scheduling algorithms for unit-time jobs are studied. The least upper-bound on the ratio of the length of the critical path schedule to that of an optimal schedule is established for an n-processor system. A sufficient condition under which the critical path algorithm is optimal is given. A variation of the critical path algorithm is considered. It is shown to produce optimal schedules when there are only two processors in the system. Finally, the successor algorithm is studied and the least upper-bound on its worst-case performance on a two-processor system is obtained.

R75-350—Cuneo, R. P., "Selected Problems of Minimization of Variable-Valued Logic Formulas" (55 pp., Technical Report UIUCDCS-R-75-726, Department of Computer Science, University of Illinois, Urbana, Illinois)

Algorithms for the minimization of variable-valued logic formulas are described. The method of implementation of these algorithms in a PL/1 program AQP is given along with a user's guide and two examples. Also included is the basic definition of the variable-valued logic system V1.

R75-351—Larson, James and R. S. Michelki, "AQVAL/1 (AQP) User's Guide and Program Description" (86 pp., Technical Report UIUCDCS-R-75-731, Department of Computer Science, University of Illinois, Urbana, Illinois)

AQVAL/1 (AQP) is a PL/1 program which synthesizes quasi-optimal formulas of the variable-valued logic system V1. By "quasi-optimal formulas" we mean here disjunctive simple V1 formulas, which are optimal or sub-optimal with regard to a fixed optimality functional. The basic application of the program is in the area of machine learning and inductive inference (inductive learning): from descriptions of objects with known class membership, the program infers optimal or sub-optimal descriptions of object classes. These descriptions are expressed as V1 formulas and represent certain generalizations of inputted information. The program can also be used (at the appropriate setting of its parameters) for an efficient minimization of binary- or multi-valued switching functions with a large number of variables (e.g., 50-100 variables).

R75-352—Sugaya, Hirotsugu, "Display of Directed Graphs for Visual Communication" (54 pp., Technical Report UIUCDCS-R-75-735, Department of Computer Science, University of Illinois, Urbana, Illinois)

The purpose of this thesis is to understand in a quantitative way what properties a picture of a graph must have in order to be easily understandable. Efficient
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